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Fluid–Structure Interaction Study of IC Stacking Chips Arrangement During Encapsulation Process

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ABSTRACT

The purpose of this study is to present the experimental and simulation studies on the influence of stacking chips arrangement for a three-dimensional encapsulation process of 3D stacked flip-chip package. A bidirectional coupling method that adopted mesh-based coupling parallel was implemented. The encapsulation process was modelled using computational fluid dynamic software (FLUENT), while structural analysis was executed using finite element method software (STRUCTURAL). The results of this investigation show that edge regions of chip deformed due to the continuous force caused by the Epoxy molding compound (EMC). Furthermore, pressure differences between upper and lower streams also caused the edge regions of chip deformed. Furthermore, The results of this study indicate that staggered arrangement significantly reduced air traps for packages due to flow on top of the chip was slightly faster when the stacking arrangement changed.

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1. Introduction

Today, the trend of integrated circuit (IC) packaging is moving in the direction of miniaturization. The cost-effective approach to increase more functions to an electronic system was to fit in more functions into the individual chips themselves. However, cost and yield issues can prevent such integration from being economically feasible [1]. With the advanced IC packaging technology, both performance and cost advantages can be achieved by splitting a single chip system into multiple dies. With this trend toward smaller and smaller structures in today advanced processes, finding and analyzing the root cause of failures and maintaining package reliability become increasingly challenging. Therefore, the IC package including the silicon chip, solder bumps, wire bonding, lead frame and passive components is protected by epoxy molding compound (EMC). The encapsulation

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process is widely used to encapsulate package components. Material selection, proper handling during the process control and an (IC) package design are vital to maintain package reliability and quality. Deformation on the silicon chip and solder bumps during encapsulation reduce the reliability of the package.

The die stacking technology has immensely progressed throughout the years, which includes side-by-side combinations of stacked die and three-or-four-die stacks within a package. The die stacking is usually executed with different die sizes so the bottom die was always larger than the top die to allow wire bonding of both. Figure 1 shows stacked packages from Amkor and Intel. Currently, it is common to see the stacking of same-size die or a larger dice over a smaller one. In stacked chip packages with conventional wire bonding, a spacer is needed to provide controlled bond line thickness, to meet wire bonding and molding tolerances for thin packages. When the number of stacking chips increases, the package requires reliable protection. Therefore, the encapsulation process is important for IC packages to increase their reliability by covering the chips and protecting them from a dangerous environment. However, during the encapsulation process, the formation of a void or air trap reduces the package reliability. This problem was discussed in several IC encapsulation processes, such as the thin quad flat package (TQFP) [2], stacked-chip scale package, mold array package (MAP) [3],ball grid array (BGA) [4] and molded underfill (MUF) [5]. During the encapsulation process, the void formation issue is vital in IC packaging. Since the need for more memory in a limited space is increasing, integration of various functions into the same package is becoming more crucial during the encapsulation process. The thickness, size, and matrix array of chips and the arrangement of stacking chips have a significant influence on mold filling yields

In the IC encapsulation process, the encapsulant is transferred to the mold cavity by using transfer-molding technology. Package encapsulation is usually done with transfer molding due to the high accuracy of transfer molding tooling and low cycle time of the process. The visualization of the encapsulation process has been restricted by Costlier and non-transparent molding tools. Therefore, a numerical simulation provides understandings and analysis into fluid-structure interaction (FSI) phenomenon in the encapsulation process. Simulation software such as PLICE-CAD [6], C-MOLD [4] ,FLUENT [7,8], Moldex3D [9] and lattice Boltzmann method [10] have been used to predict and improve reliability various types of IC packages. Various studies have reported on the use of the finite volume method (FVM) and the finite-element method (FEM) integrated with mesh-based parallel code coupling interface (MpCCI) for flow analysis and structure analysis [11–13]. However, to the best of our knowledge, a report on the application of FSI for the stacked chips is still lacking in the experimental work. The visualization of the FSI phenomenon in the actual package is difficult because of the limitations of package size, available equipment, and the high cost of the experimental setup. However, experimental data are necessary to validate the simulation results in the FSI analysis of stacked flip chip packaging.

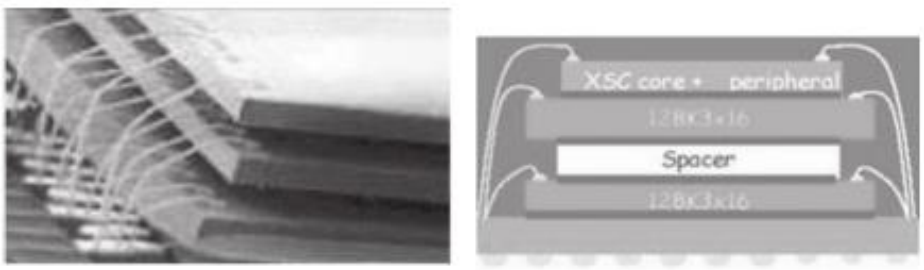

Fig. 1. Stacked packages from Amkor and Intel [14]

A limited amount of literature has been published on the study of chip stacking. The investigation on fluid-structure interaction (FSI) analysis on the effect of outlet vent arrangement during the encapsulation process of the plastic ball grid array (PBGA) packaging was accomplished by Ramdan *et al.,* [15]. The results show the four outlet vent arrangement is found to be lower on the wire deflection compared to the two outlet vent. Ong *et al.,* [16] studied the effect of stacking chips package with through silicon via (TSV) during the encapsulation process. The study has found out that higher displacement is anticipated at the top part of TSV. However, higher Von Mises stress is anticipated at the bottom part of TSV. Besides that, Ng, *et al.,* [17] the effect of temperature on the underfill of the multi-stack ball grid array. Their findings show that the application of thermal delta significantly decreases the filling time through the multi-stack packages. The research objective in all the above is that almost all involve stacking chips, but the bidirectional fluid structure fluid-structure interaction (FSI) behaviors of the of 3D stacked flip-chip package on the effects of stacking arrangement have not been investigated in the literature.

The present study focuses on the effect of die stacking arrangement with fluid-structure interaction approach during mold filling. The ANSYS is used as tools to carry out the FSI for the simulation model of the package. The Castro-Macosko and Kamal models are used to describe the non-Newtonian behavior and the curing kinetics of the epoxy molding compound (EMC). The volume of fluid (VOF) [18] is applied to track the melt front advancement in FLUENT. Flip chip is defined as FSI structures in Structural. ANSYS System Coupling is employed to connect FLUENT and Structural programs by exchanging data between them. This implementation enables the visualization of the real-time interaction between the fluid and the structure in the molded packaging for different layouts

2. Methodology

In the fluid flow analysis, the continuity equation, Navier-Stokes equation and energy equation are taken into account for describing the EMC flow by considering the fluid as incompressible. The equations are solved in the simulation (FLUENT) as listed below.

Continuity equation

$$\frac{\partial \rho}{\partial t} + \frac{\partial}{\partial x_i}(\rho u_i) = 0 \tag{1}$$

The conservation of momentum is described by:

$$\frac{\partial}{\partial t}(\rho u_i) + \frac{\partial}{\partial x_i}(\rho u_i u_j) = -\frac{\partial P}{\partial x_i} + \frac{\partial \pi_{ij}}{\partial x_j} + \rho g_i + F_i \tag{2}$$

The conservation of energy can be expressed as:

$$\frac{\partial}{\partial t}(\rho h) + \frac{\partial}{\partial x_i}(\rho u_i h) = \frac{\partial}{\partial x_j}\left(k \frac{\partial \pi_{ij}}{\partial x_i}\right) + \eta \dot{\gamma} \tag{3}$$

where, P is the fluid pressure, πij is the stress tensor and g_i and F_i are the gravitational acceleration and external body force in the i direction, respectively, T is the temperature, k is the thermal conductivity, η is the viscosity and $\dot{\gamma}$ is the shear rate.

The temperature in the encapsulation on the fluid flow can be expressed using the energy equation:

$$pC_p\left(\frac{\partial T}{\partial t}+u.\nabla T\right)=\nabla(\mathrm{k}\nabla T)+\ \Phi \tag{4}$$

where the energy source term is:

$$\Phi=\ \eta\dot{\gamma}+\dot{\alpha}\Delta H \tag{5}$$

Castro–Macosko model is employed to describe the non-Newtonian behavior of the EMC. This viscosity model incorporates the dependence on curing, strain rate, and temperature and can be written as:

$$\eta(T,\dot{\gamma},\alpha)=\frac{\eta_o(T)}{1+(\frac{\eta_o(T)\dot{\gamma}}{\tau^*})^{1-n}}\left(\frac{\alpha_g}{\alpha_g-\alpha}\right)^{C_1+C_2\alpha} \tag{6}$$

Where

$$\eta_o(T)=B\exp\left(\frac{T_b}{T}\right) \tag{7}$$

where η is the viscosity at temperature T, γ is shear rate, α is the degree of cure, η_o is zero shear viscosity, n is power law index, τ* is a shear constant, α_g is the degree of cure at gel point, and C1, C2, B, and T_b are the fitted constants.

The equation used to predict the rate of chemical conversion of material [6] can be expressed as:

$$\frac{d\alpha}{dt}=(k_1+k_2\alpha^{m_1})(1-\alpha)^{m_2} \tag{8}$$

$$k_1=A_1exp\left(-\frac{E_1}{T}\right)\text{ and }k_2=A_2exp\left(-\frac{E_2}{T}\right) \tag{9}$$

where E_1 and E_2 are activation energies, A_1 and A_2 represents the Arrhenius pre-exponential factors, m_1 and m_2 describes the reaction order, and T is absolute temperature. These viscosity and curing models have been used by many scholars [19–23].

The bidirectional fluid-structure coupling proposed here is achieved by using the ANSYS Multi-field® solver. In this solver, the structural analysis is solved using ANSYS Mechanical whereas the fluid analysis is calculated using ANSYS FLUENT. The results of analysis produced from the ANSYS FLUENT were transferred to ANSYS Mechanical during FSI analysis. Real-time analysis data were exchanged from one solver to the other. The forces induced from the fluid acting on the chips surface were directly solved by ANSYS Mechanical during the interaction. Therefore, the bending of the chips was computed instantaneously. During the FSI simulation, the chips were defined as the coupled regions. FLUENT solver was utilized to examine the fluid flow modeling by simulating the physics of the flow front that fed into the cavity. The displacement, von Mises stress, and shear stress of chips during the encapsulation process was computed by ANSYS Mechanical solver. The real-time analysis of FSI simulation is shown in Figure 2.

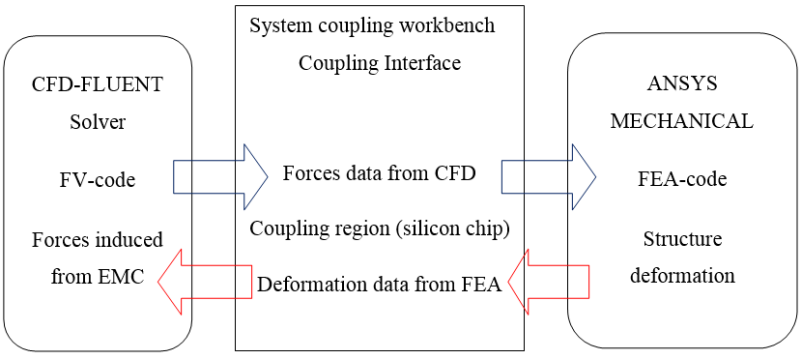

Fig. 2. Flow chart exchange data real time coupling

3. Methodology

ANSYS FLUENT was used to model the mold package with two different arrangements of stacked chips. The two different arrangements were considered for the simulation as shown in Figure 3. For the present study, a single inlet and outlet scheme was used with designed height and width (80mm x 80mm x 2.3mm). Figure 4 shows the parameters and components for 4 stacked chips package used in the analysis. The gap height between top surface of silicon chips and mold wall was set as 0.1 mm and constant for all cases. The structures (silicon die and spacer) were placed at the middle of the mold to control the peak pressure. The package models were optimized and meshed by using ICEM software with 470,000 to 500,000 hexahedral elements prior to the simulation analysis. The meshed model with boundary condition setup is shown in Figure 5.

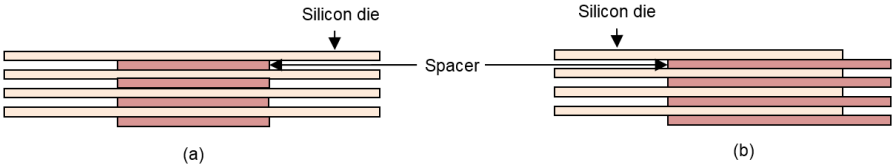

Fig. 3. Two types of multi-stacking-dies arrangement (a) Uniform and (b) Staggered

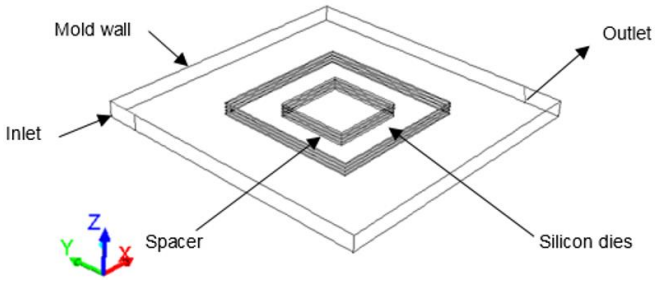

Fig. 4. Isometric view of 4 stacked chips package for uniform arrangement

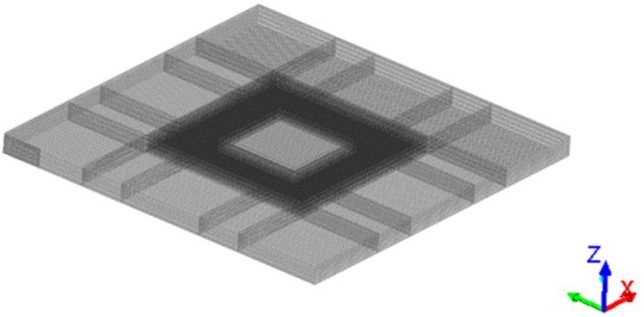

Fig. 5. Meshed model for FLUENT analysis of uniform arrangement

In FLUENT, there are two phases in the model were considered, namely as EMC and air. In each computational cell single momentum equations were shared by the fluid and the volume fractions of the fluid. The VOF scheme model was used to track the melt flow front of the multiphase model. The EMC used for this study is Hitachi CEL9200 and its material properties are shown in Table 1. A user-defined function (UDF) script was written in C++ language in order to integrate the Castro-Macosko viscosity model with curing kinetics using Microsoft VISUAL Studio 2010 and compiled in FLUENT program to solve the viscosity model. In FLUENT code, A COUPLED algorithm was applied for pressure–velocity calculation. In each time step for the volume fraction, implicit solution and time dependent formulation were considered. In the analysis, the optimum time step size of 0.001 was used. A constant 1 MPa inlet pressure with preheat temperature of 90 °C was used in the mold setup. The mold temperature (T_w) was set to 150 °C. The dynamic mesh considering of layering/remeshing zone was enabled for the FSI simulations, and second-order upwind was applied for the momentum, volume fraction, and energy equations. The analysis consumed around 20 hours to complete one case.

Table 1
EMC material properties used in FLUENT simulation [24]

Castro-Macosko model parameters	
B (Pa.s)	$1.624e^{-7}$
T_b (K)	11620
C_1	3.338
C_2	0.2824
α_g	0.4447
Kamal model parameters	
m_1	0.4925
m_2	1.117
A_1 (s−1)	29730
A_2 (s−1)	$4.836e^{6}$
E_1(k)	25330
E_2(k)	8443

ANSYS Mechanical Structural was utilized to create the structures (silicon dies, and spacers) and execute the structural analysis. The structures were built based on the real scale dimensions given in Table 2 and meshed using a hexahedral scheme with a total of 20,829 elements. During the molding process, the rigid stacked chip is clamped and fixed in the mold. In the modelling, the substrate effects were ignored. FSI structure was coupled at the silicon die and the bottom surface of spacer was set as fixed in boundary condition setup (Figure 6). The mechanical properties of the silicon are constant for all cases and were summarized in Table 3.

Table 2
Dimensions for silicon die and spacer used in all models (H=height, W=width, T=thickness)

Arrangement type	Uniform (H x W x T)	Staggered (H x W x T)
1st layer silicon die size(mm)	10 x 10 x 0.1	10 x 10 x 0.1
2nd layer silicon die size(mm)	10 x 10 x 0.1	10 x 10 x 0.1
3rd layer silicon die size(mm)	10 x 10 x 0.1	10 x 10 x 0.1
4th layer silicon die size(mm)	10 x 10 x 0.1	10 x 10 x 0.1
Spacer size(mm)	5 x 5 x 0.15	2.5x2.5x 0.15

Table 3
mechanical properties of structures[24]

Arrangement type	Imitated chip	Imitated spacer
Elastic modulus, E (GPa)	1.57	2.7
Poisson ratio, v	0.37	0.375
Density, p_s (kg/m^3)	1180	1170

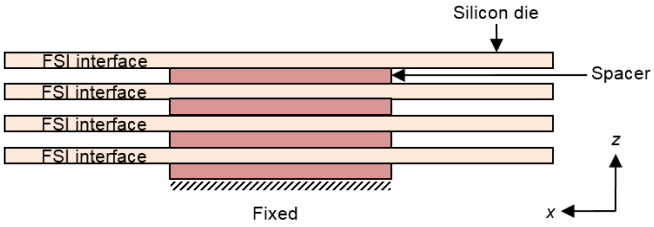

Fig. 6. Boundary conditions for structural solver

4. Results

4.1 Grid Independence Test

Grid independence test was carried out to examine the stability of the mesh resolution used in the simulation and recognize the optimum mesh for a precise computational result. This test typically performed for the simulation analysis in order to find the adequate number of mesh elements. The simulation was evaluated through the range of mesh from low to the extra fine. The results of the different number of mesh was compared with highest number of mesh sizes (Table 4). From the data analysis results, the optimum mesh is the mesh resolution that compromise discretization error within 5% standard limit. As Table 4 shows, the optimum mesh grid utilized in this study is the fine mesh (mesh model 5) with 470,564 total number of cells. This mesh grid is chosen due to to the optimal simulation's accuracy and low execution time.

Table 4
Summary of grid independence test

Mesh model	Grid resolution	Number of cells	Volume % at 90% of filling time	Discretization error (%)
1	low	81435	90.98	10.56
2	Medium	179997	89.05	8.21
3	Medium	264656	88.12	7.08
4	Fine	355202	86.88	5.58
5	Fine	470564	82.77	0.58
6	Extra Fine	610536	82.29	–

4.2 Fluid Structure Interaction

In the present study, FSI modelling was performed. Figure 7 shows the FSI simulation results from ANSYS FLUENT and Structural solver for uniform arrangement. The flow front profile is depicted in the left column while the right column shown the deformation of the structure. Top and front views are used to analyse the structure deformation. In the Structural column, D represents displacement during the filling process. Deformation of the silicon chip is defined as a change in shape due to the induced forces during the encapsulation process. Displacement is the value measured in the deformation mode. The imitated chip began to deform around the edge at 0.5 s filling time from the first interaction. The continuous flow from the inlet covered nearly 50% of the chip at 1.5 s. Nonetheless, at 1.5 s to 2.2 s filling time, the fluid covers totally 50% to 80% of the chip. Hence, the downward deformation of the stacked chip around the edge is observable at the front view of the chip at 1.2 and 3 s. When the EMC flow front reached the middle of the chip at 1.2 s, the red region shifted to the chip edge, thus indicating a more critical downward displacement at the chip edge. At 2.8 s, an identical magnitude of vertical displacement was noticed. This displacement pattern happened when the EMC flow front flowed pass through all the stacked chips.

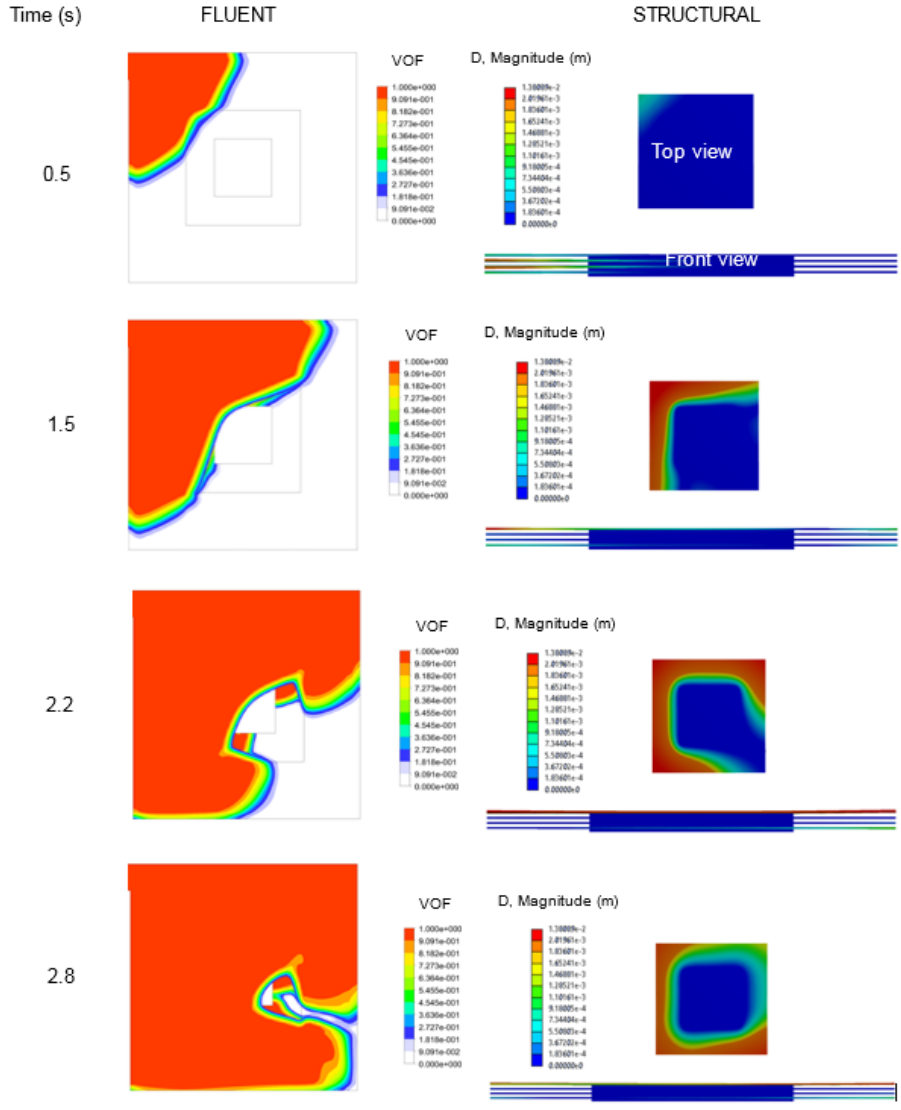

Fig. 7. FSI simulation for uniform arrangement

In addition, staggered arrangements were also carried out for the FSI simulation as shown in Figure 8. It was found that stacking chip arrangement have an influence on the chip deformation. This is unlike the occurrence noticed at the uniform arrangement (Figure 7). There is less red region on the chip edge which indicates a less critical downward displacement. The downward displacement was concentrated at the side of the chip. It can be concluded that the staggered arrangement of the spacer provided better support to the silicon chip in molded packages. The staggered arrangement was found to reduce the displacement of the chip, therefore, it decreased the undesirable defects and maintained the reliability of the package.

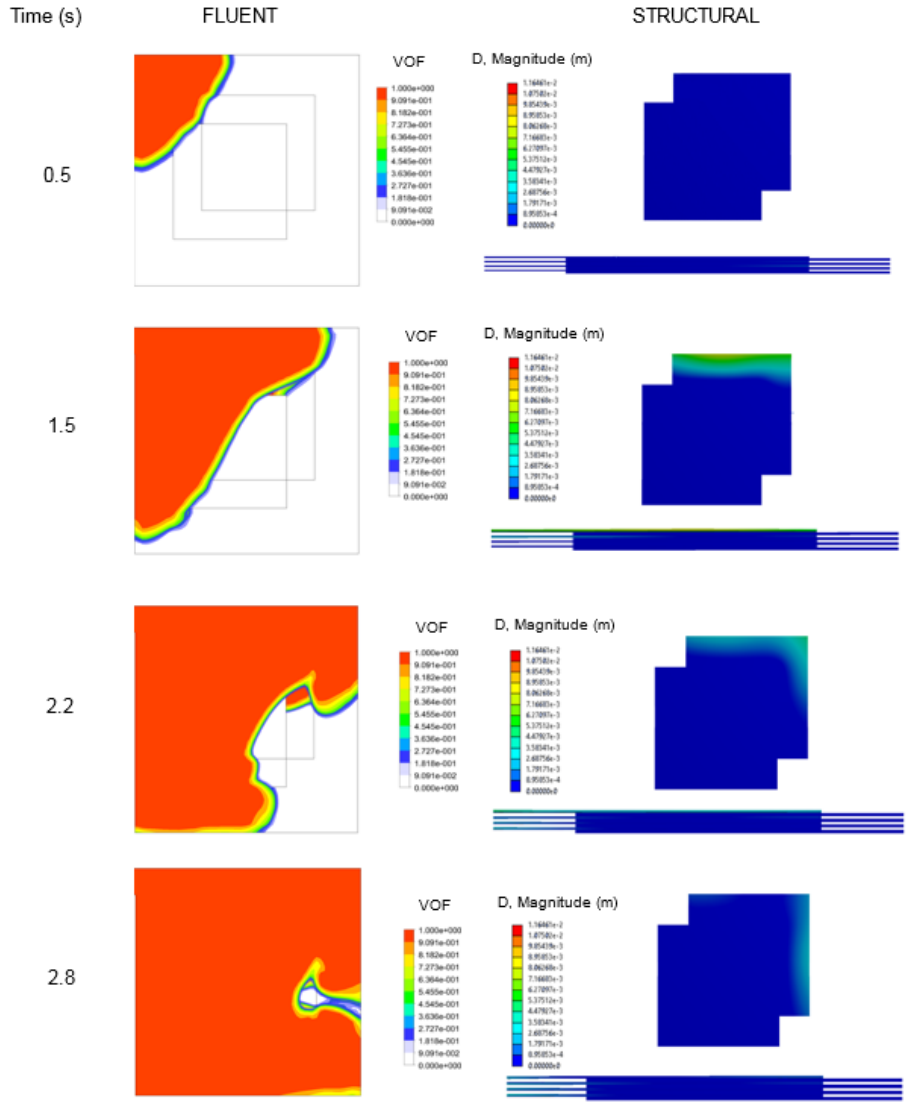

Fig. 8. FSI simulation for staggered arrangement

4.3 Void Formation

The current FSI simulation predicted the void formation during the encapsulation process. In this section, the influence of stacking chips arrangement was investigated on 3D stacked flip- chip packaging. Figure 9 depicted the top and bottom views of the 3D stacked flip-chip package for uniform and staggered at a short shot of 3.0 s. The results show the formation of air traps in the package during the filling process. The pointed area volume fraction was equal to zero or less one which indicated the air phase. The void concentration between the uniform and staggered

arrangement were compared. The application of the staggered stacking arrangement, as shown in Figure 9 (b), yielded better filling around the corner regions compared with the uniform stacking arrangement, as shown in Figure 9 (a). However, for both arrangements, the void of the package was recognized in the regions between the stacked chips and spacer and in the portion close to outlet gate. Knit line formed at the top and bottom of the package due to the high resistance of EMC flow in the space between the stacking chips, and the interface between separate flows. These findings of the current study are consistent with those of Schreier-Alt *et al.,* (2011) [3] who found that the knit line caused the void in their experimental analysis for Mold Array Package (MAP).

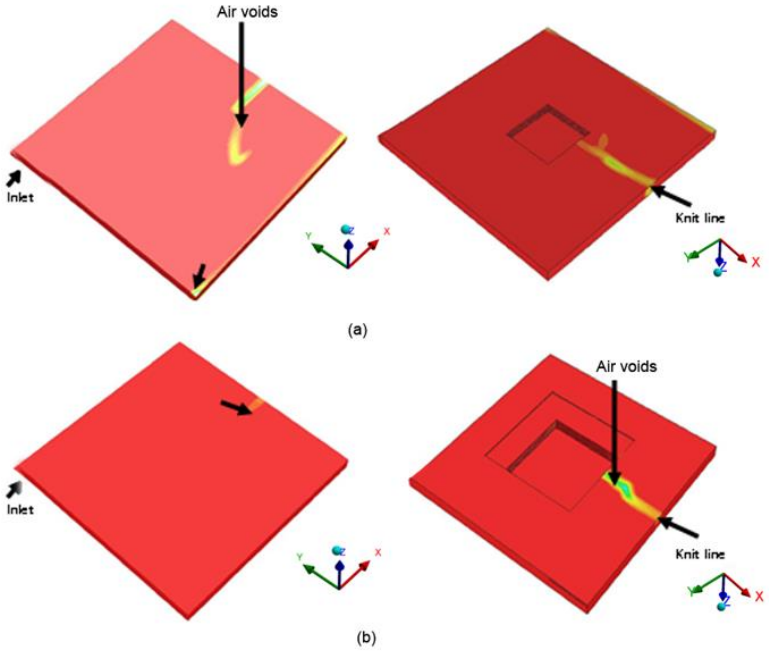

Fig. 9. Top and bottom views of stacking chips arrangement (a) Uniform (b) staggered

The effect of the stacking chips arrangement created different void concentrations during encapsulation process. Figure 10 shows the percentage of void formation of different stacking arrangement types in chips package. The uniform arrangement type had the lowest percentage of void (1.8%), followed by the staggered arrangement type (2.6%), respectively. The difference between percentages of the void was 0.8%. Although the staggered arrangement type had a higher void than the uniform arrangement type, it provided the proper filling around the corner and edge regions of the package. Therefore, the void may cause crack propagation to the encapsulated IC chip. Consequently, the stacking chips arrangement significantly affects the void formation in the 3D stacked flip-chip packaging.

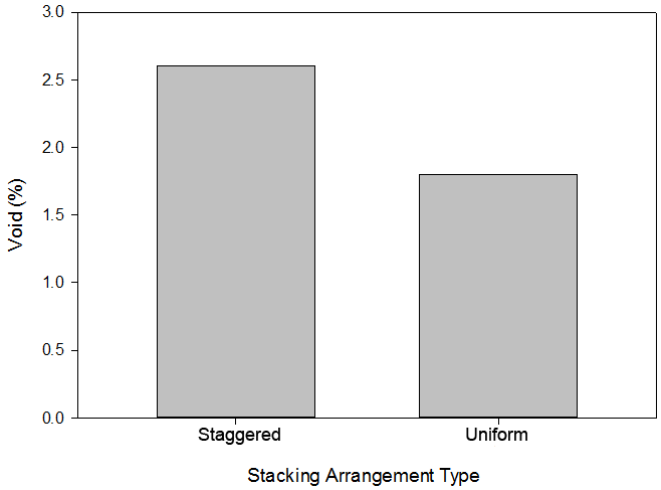

Fig. 10. Percentage of void formation of different stacking arrangement types in chips package

4.4 Analysis of Stress in Packaging

The stress of the component structures is difficult to determine, especially for small size IC packaging. To overcome this problem, the FSI simulation method was introduced to handle the estimation and modeling of complex design in the structural analysis. This technique is important for the continuous improvement in microelectronic reliability problems.

The von Mises stress of the stacked chip for uniform arrangement during the filling process is depicts in Figure 11. The flow from fluid generated a force on the structure and caused stress on the chips. The results of this study indicated that the stress distribution was affected by the fluid force which corresponded to the interaction between the EMC and the silicon chip. At 1.4s, the concentration of stress was maximum at the intersection between the imitated chip and the spacer. When the filling process almost complete (2.8s), the concentrated stress point shifted to the opposite point at the joint between the imitated chip and the spacer. The stress subjected to the silicon chip was reduced when the mold was filled by the EMC. This trend was discovered at the final filling stage (0.5-2.8s). The von Mises stress displayed different distribution trends when the stacking chip arrangement is changed as shown Figure 12. The allowable von Mises stress is less than 500MPa. The increased solder bump count minimized the effects of the solder bump shape during encapsulation. The stress was distributed at the edge of imitated chip, which was supported by spacers, and was found to be higher than other regions. Based on a comparison of Figure 11 and Figure 12, uniform stacking chips arrangement yielded higher von Mises stresses to the silicon chip compare to staggered stacking chips arrangement. Unsuitable process control could cause unexpected situations such as deformation, overstress, and 'swept away' phenomenon [25] in the IC packaging. Therefore, the FSI phenomenon during encapsulation for miniaturized, thinned chip, and 3D packaging and integration should be considered in the process.

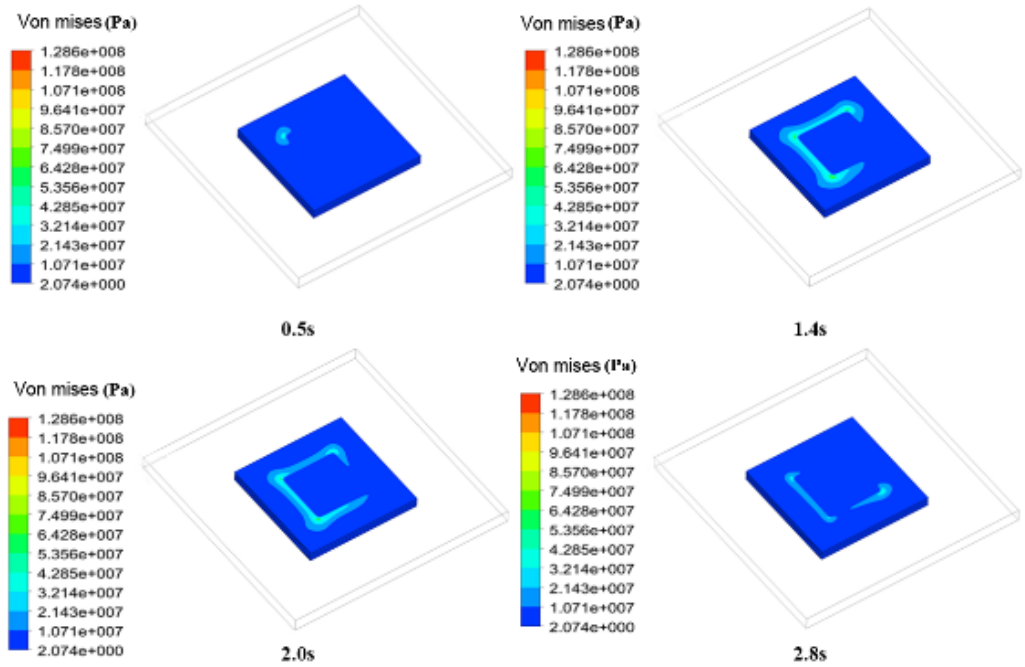

Fig. 11. Von Mises stress of the imitated chip for uniform arrangements

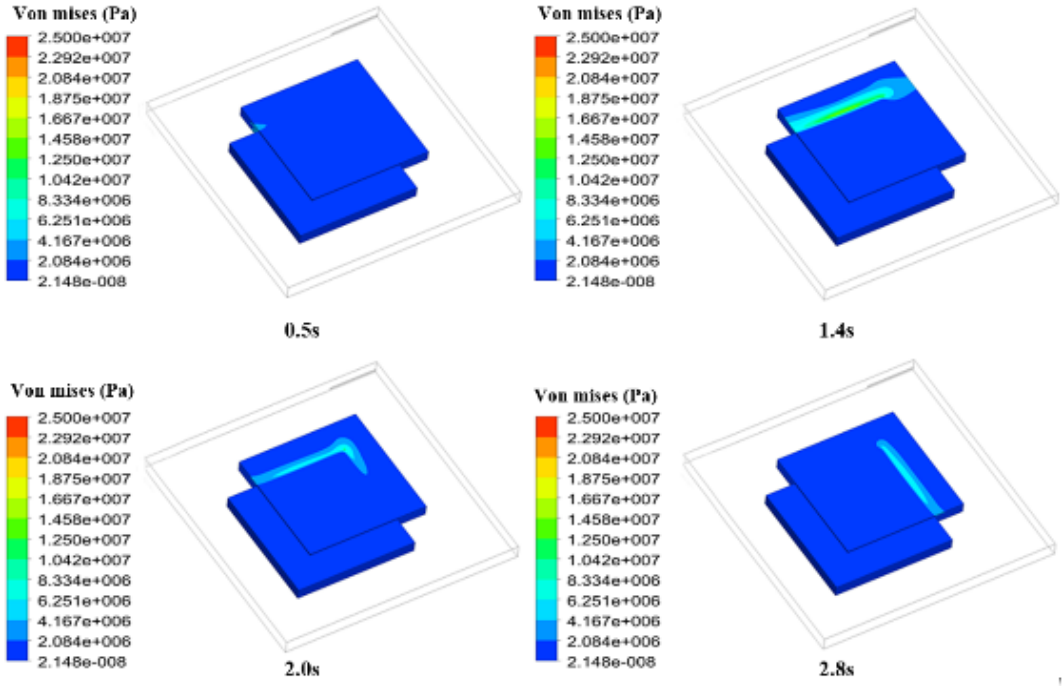

Fig. 12. Von Mises stress of the imitated chip for staggered arrangements

Figure 13 presents the different filling stages of encapsulation process for the maximum stress parameter. The maximum stresses during filling and at the final filling stages were determined at different arrangement types. The stresses subjected to the staggered arrangement types was lower than uniform arrangement types. Therefore, the application of the staggered arrangement types effectively minimized the stress concentration on the silicon die.

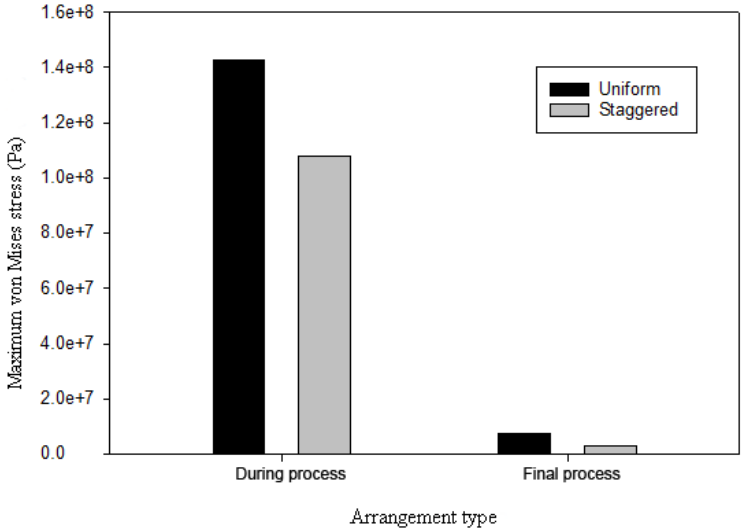

Fig. 13. Maximum von Mises stress on the chips at the ''during'' and ''final' at the ''during'' process stages

5. Conclusions

The influence of stacking chips arrangement in 3D stacked flip-chip packaging during the encapsulation process was investigated using fluid/structure interaction simulation and experiment. The bidirectional coupling method yielded results that were close to experiment. Mechanism of the void formation and fluid/structure interaction was the focus in the encapsulation experiment. The results show good agreement between simulation results and experimental data in terms of filling percentage. Overall, the filling percentage of the numerical simulation and test measurement have the same trend, which shows that the flow field calculation could accurately predict the encapsulation process.

Deformation of the imitated chip was investigated for uniform and staggered type. This results of this investigation show that edge regions of chip deformed due to the continuous force caused by the EMC. Furthermore, pressure differences between upper and lower streams also caused the edge regions of chip deformed. The void formation mechanism was also investigated at a uniform and staggered arrangement type. The results of this study indicate that staggered arrangement significantly reduced air traps for packages due to flow on top of the chip was slightly faster when the stacking arrangement changed. Thus, the current research offered superior visualization and knowledge of the FSI occurrence during the process. Additionally, the FSI simulation approach provides realistic predictions on the flow front, structural deformation, stress and void formation to resolve the FSI issues in the actual packaging process.

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