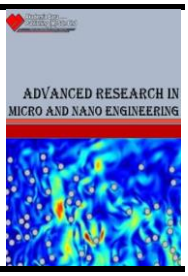
Penerbit Akademia Baru

Journal of Advanced Research in Micro and Nano Engineering

Journal homepage:
https://www.akademiabaru.com/submit/index.php/armne/index
ISSN: 2756-8210



Direct-Written Silver Electrodes for All-Solution-Processed Low-Voltage Organic Thin Film Transistors Towards Flexible Electronics Applications

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ARTICLE INFO

Article history:
Received 19 April 2024
Received in revised form 21 May 2024
Accepted 24 June 2024
Available online 30 July 2024

Keywords:
Organic thin film transistor; direct-write printing; TIPS-pentacene; PVA; low-voltage; semiconductor devices

ABSTRACT

Recent progress in printed electronics has offered the possibility of fabricating various organic-based electronic devices, such as organic light-emitting diodes (OLEDs) and organic thin film transistors (OTFTs). As one of the important deposition methods in printed electronics, an inkjet printing technique offers the deposition of solution-processable materials onto a variety of substrates using simpler fabrication steps at lower processing temperatures, which is suitable for flexible electronic applications. Despite being the leading choice in OTFT fabrication, the clogging issues that frequently occurred at the printhead nozzle have not only limited the material selection but also restrained the efforts to bring organic electronic devices to the market. Apart from that, although remarkable progress has been made to enhance the performance of the OTFT, the high operating voltage resulting from the low gate capacitance density of the inorganic oxide-based dielectric layer remains a critical limitation that hinders the practical application of the OTFT. Hence, in this paper, we propose a simple solution-based method to develop a low-voltage OTFT. This work utilized a direct-write printing technique to print silver source/drain and gate electrodes incorporated into a bottom gate bottom contact OTFT structure, a spin-coating deposition method to deposit both small molecule TIPS-pentacene organic semiconducting layer and high-*k* PVA dielectric layer. Notably, the proposed OTFT achieved a micrometre channel length with a saturation mobility of 4.49×10^{-1} cm^2/Vs, a threshold voltage of -1.5 V, an on/off current ratio of 10^8, and a subthreshold swing of 66.8 mV/dec while the overall fabrication temperature and operating voltage are kept below 150 °C and -15 V, respectively. The direct ink writing technology incorporated into the high-*k* dielectric layer provides a new strategy to fabricate organic-related components, particularly the OFTFs at lower manufacturing cost and temperature towards flexible and low-operating voltage electronic devices.

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https://doi.org/10.37934/armne.21.1.7588

1. Introduction

Recently, electronic devices based on solution-processable organic materials have gained substantial attention due to their potential applications in sensors, displays, wearable, and flexible electronics applications, as reported in [1-4]. As one of the backbones of organic electronics, organic thin-film transistors (OTFTs) show competitive benefits against their inorganic silicon-based transistors, which include low processing temperature, low cost, and notable mechanical flexibility. Besides, the OTFTs possess a simpler fabrication process that eliminates the need for high temperature and high vacuum deposition processes, as well as sophisticated photolithography patterning techniques, making them suitable for the production of flexible and low-cost wearable electronics. Thanks to their compatibility with various deposition and patterning techniques such as screen printing, inkjet printing, and spin-coating techniques, the OTFTs can be fabricated conveniently without compromising their electrical performance.

The OTFT is commonly made up of three main functional layers which are the organic semiconducting layer, the dielectric layer, and the electrodes (i.e., source, drain, and gate terminals). Figure 1 depicts the schematic diagram of a bottom gate bottom contact OTFT. The choice of materials and the compatibility between materials play an important role in the OTFT performance, as stated by Yusof *et al.,* [5]. Thus, careful consideration of material selection should be taken during device fabrication.

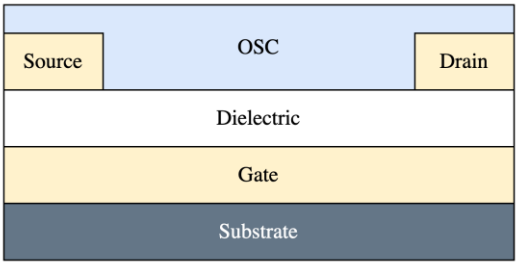

Fig. 1. Schematic diagram of a bottom gate bottom contact OTFT

The organic semiconducting layer governs the charge transport; hence, it dictates the performance of the OTFT in terms of the charge carrier mobility. Currently, molecule-based semiconductors, including small molecules and conjugated polymers, are used as an organic semiconducting layer. Although both small molecules and conjugated polymers are solution-processable materials, the latter show poor performance due to their natural susceptibility towards oxygen in the inert condition, as proven by Kehrer *et al.,* in [6]. Besides that, Sawatzki-Park *et al.,* [7] in their work mentioned that the formation of polymeric thin film is rather complex and has not demonstrated promising performance yet. Small-molecule OTFTs, on the other hand, have shown better performance, both electrically and morphologically. Among the small-molecule materials, 6,13(bis-triisopropylsilylethynyl) pentacene (TIPS-pentacene) has been used extensively by researchers due to its relatively high carrier mobility and air stability [4,8–10].

A low operating voltage OTFT can be realized by increasing the gate capacitance. The gate capacitance can be defined as the gate capacitance of the gate terminal of the OTFT and can be expressed as Eq. (1), which can be found in [11]

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{1}$$

Where C is the gate capacitance, ε_0 is the vacuum permittivity (8.86×10^{-12} C^2 N^{-1} m^{-2}), ε_r is the dielectric permittivity, A is the plate overlap area, and d is the distance between the two plates. From the equation, the capacitance varies directly with ε_r (which is also known as dielectric constant, k) and inversely proportional with d. Two common ways can be considered to increase the gate capacitance C; first, by using high dielectric constant k materials and second, by decreasing the dielectric thickness d as highlighted in [12,13]. Nonetheless, scaling down the dielectric thickness is impractical since it triggers a high leakage current, eventually degrading the overall OTFT performance. Due to this reason, the first option seems to be more viable to increase the gate capacitance of the device in order to achieve a low operating voltage OTFT.

The amorphous, thermally grown silicon dioxide (SiO_2) has been widely used to fabricate the OTFT thanks to its stable characteristics, both thermodynamically and electrically, high-quality interface, especially with the silicon substrate, and excellent electrical isolation properties [14,15]. Despite its fascinating advantages, this material is, however, incompatible with flexible electronic applications. This is because an extremely high temperature between 700℃ to 1300℃ during the thermal oxidation will break down the flexible substrate. To overcome this problem, researchers started to use solution-processable organic materials for dielectric layers. Due to its high-*k* properties, eco-friendliness, as well as biocompatibility, polyvinyl alcohol (PVA) has gained popularity among researchers to be implemented as the gate dielectrics as reported in [16–18]. On top of that, PVA shows good flexibility, which is necessary for stretchable electronic implementation, as shown in [19].

Various printing techniques have been explored for the fabrication of flexible electronics, either by contact (e.g., screen printing and flexography) or non-contact (e.g., inkjet printing and direct-write printing) methods. Among the available options, the non-contact inkjet printing method has been the most promising technology and gained its popularity as it does not require a vacuum environment during the fabrication process reduces material wastage through drop-on-demand technology, and scalability to large-area manufacturing as mentioned in [20–22]. In addition, due to the contactless and direct patterning of the functional layers, electrical and morphological damage on the other functional layers induced by developing and etching processes could be avoided, as stated in [23].

Regardless of its benefits, the inkjet printing technology has several drawbacks that hinder the process of bringing OTFTs into the market. Tao *et al.,* [21] and Martinelli *et al.,* [24] mentioned that the clogging issues and the stringent requirements of both the conductive inks (i.e., low viscosity ink typically between 1-25 mPa s) and substrate states (i.e., low surface tension between 20-50 $mN.m^{-1}$) remained challenges in the inkjet printing technology. Thus, to counter these issues, a direct ink writing (DIW) technique has been explored to fabricate the OTFTs.

Similar to the inkjet printing technique, the DIW method uses a nozzle to deposit the ink onto a substrate. The ink can be conductive materials (e.g., nanoparticle-based and flake-based silver inks) as well as composed of polymers suspended or solubilized in the solvents which are not restricted to the low viscosity materials as in the inkjet printing as recommended in [24–26]. On top of that, this method does not require high processing temperatures, hence making it suitable for flexible electronic applications. Although the DIW method has been used to deposit the electrodes for several electronic components such as diodes and light-emitting diodes (LEDs), as reported by Hou *et al.,* [27], nevertheless a limited number of research can be found in utilizing this method for the fabrication of the OTFTs. Since a wide range of materials can be used in the DIW printer, therefore, this technique can offer layer-by-layer patterning directly from a computer-aided design (CAD) and can serve as a new bottom-up manufacturing technology to fabricate electronic devices. The general steps in the manufacturing process of the DIW printing technique can be represented as shown in Figure 2.

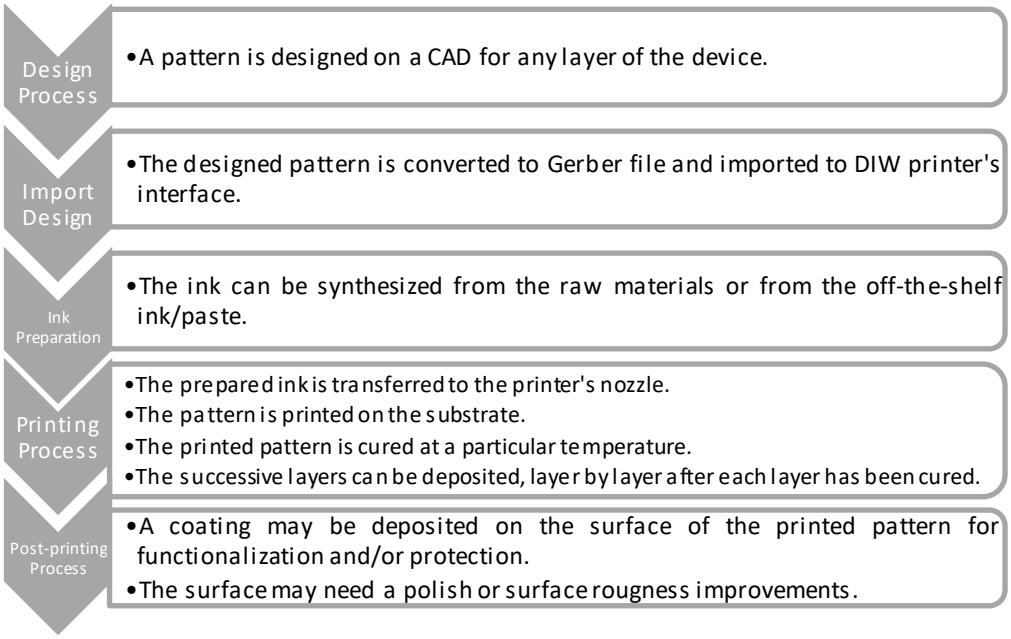

Fig. 2. General steps in the manufacturing process of the DIW printing technique [28]

In this work, we successfully reported a low-voltage, room-temperature, printed, and all-solution-processable OTFT using silver conductive ink, PVA, and TIPS-pentacene as the conductive electrodes, gate dielectric, and organic semiconducting (OSC) layers, respectively on the silicon wafer. Interestingly, the electrodes were deposited using the DIW printing technique up to a micrometre channel length. Besides, the proposed OTFT showed a significant improvement in terms of the operating voltage since high-*k* PVA has been utilized as the dielectric layer. On top of that, the overall processing temperature has been kept below 150 ℃ to ensure its compatibility with flexible substrate requirements.

The rest of the paper is structured as follows: Section 2 specifies the materials used and experimental details in fabricating the proposed device. This section also describes the electrical and morphological characterizations of the fabricated BGBC OTFT. Next, Section 3 analyses the morphological and electrical characteristics of the fabricated device fabricated devices. These results have been discussed comprehensively and compared with previous works if applicable. Finally, Section 4 concludes the paper.

2. Materials and Experimental Details

2.1 Materials

In this research, an off-the-shelf silver conductive ink purchased from Voltera Inc., was used to deposit the electrodes (i.e., source, drain, and gate terminals), while a 99 +% hydrolyzed polyvinyl Alcohol (PVA) (M_w = 89000-98000) purchased from Sigma-Aldrich was used as the dielectric layer. For the organic semiconducting (OSC) layer, a high purity >99.9 % 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) and its solvent, 99.5 % AR Grade Toluene were purchased from Ossila Ltd., and Chemiz (M) Sdn. Bhd., respectively. All materials were used without any further purification. A single-side polished <100> silicon substrate of 625 $\pm$ 25 µm thickness and 0.001 ~ 0.003 Ω resistance acquired from Fuleda Technology served as the substrate for the OTFT fabrication.

2.2 Experimental Details

In general, this work can be divided into two main parts – device fabrication using the DIW printing technique, followed by the electrical and morphological characterizations of the fabricated device. The fabrication and measurements were conducted under ambient air and at room temperature. Note that, in this work, all solution-processable materials were used to fabricate a bottom gate bottom contact (BGBC) OTFT.

2.2.1 Fabrication of the low-voltage all-solution processable OTFT

First, the silicon (Si) substrate was diced into a 20 mm × 15 mm piece and cleaned by a standard solvent-cleaning procedure by using acetone, isopropyl alcohol (IPA), and deionized (D/I) water sequentially in an ultrasonic bath for 3 min each. The cleaned substrate was then dried using a dryer to remove any residual solvent and moisture. In this work, a Voltera's V-one DIW printer was used to deposit the gate as well as the source/drain electrodes. The conductive ink was transferred to the printer's nozzle to initiate the printing process. The printer's parameters, such as the kick and the rheological setpoint were adjusted as in the work by Yusof *et al.,* in [29]. Next, the gate electrode was deposited onto the substrate. Subsequently, the printed electrode was sintered on the printer's heated bed at a temperature between 100 ℃ to 150 ℃ for 1 hour. To deposit the dielectric layer, PVA powder was dissolved in the D/I to form a PVA solution. 100 µl of PVA solution was spin-coated on the gate electrode, followed by the annealing process at a temperature between 80 ℃ to 100 ℃ for 1 hour. To form a bottom contact device, the source/drain electrodes were printed on the PVA dielectric layer before they were cured at 100 ℃ to 150 ℃ for 1 hour. Next, to complete the OTFT structure, 60 µl of OSC solution was spin-coated on the source/drain electrodes and annealed at a temperature between 80 ℃ to 100 ℃ for 10 min to remove any access solvent. The OSC solution was prepared by dissolving TIPS-pentacene in its solvent, Toluene. Finally, any excess semiconductor on the sample's surface was cleaned with a cotton bud wetted with Toluene. Figure 3 illustrates the overall fabrication steps of the proposed low-voltage BGBC OTFT.

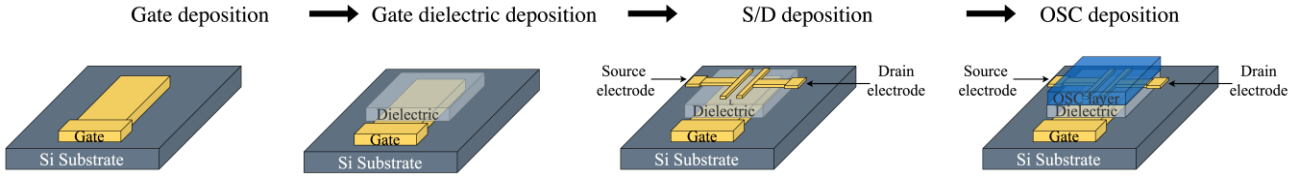

Fig. 3. The overall fabrication steps of the proposed low-voltage BGBC OTFT

2.2.2 Electrical and morphological characterization of the low-voltage OTFT

The OTFT was characterized and analyzed using a Keithley 4200 semiconductor analyzer and a quick test system consisting of a custom probe station and optical microscope. The output characteristics were measured using a V_{DS} sweep of 0 to -3 V for a range of V_{GS} values over 0 to -10 V. The investigation of the morphology of TIPS-pentacene film on the PVA/Si substrate was performed using scanning electron microscopy (SEM). The DIW printed Ag electrode surface profile was measured by a KLA-Tencor Alpha-Step® D-100 profilometer, and its morphology was characterized by a confocal laser scanning microscope (LSM) and SEM. The overall fabrication and characterization flow is depicted in Figure 4.

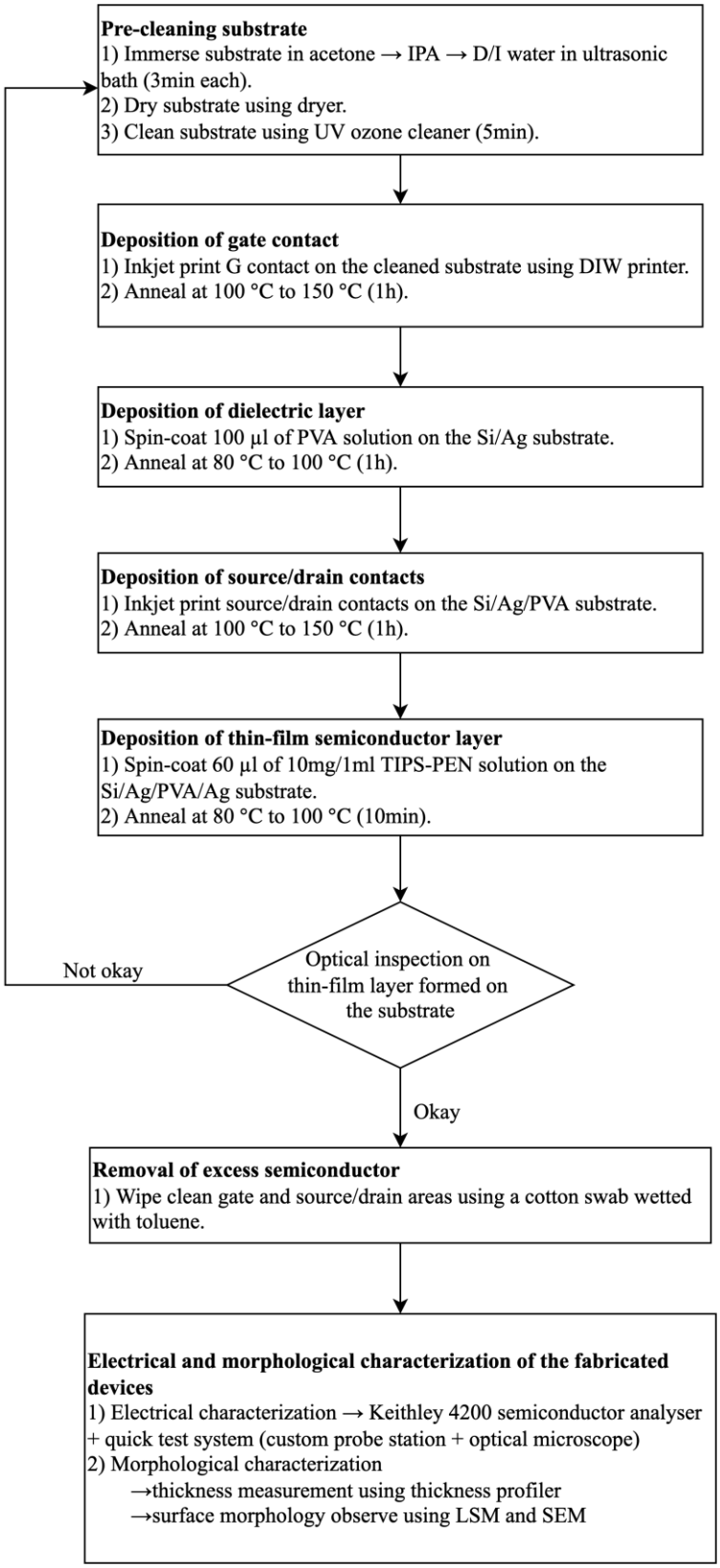

Fig. 4. The overall fabrication and characterization processes of the OTFT

3. Results & Discussion

3.1 Morphological Characterization of the OTFT

Figure 5(a) shows the schematic diagram of the proposed OTFT device based on the materials used on each layer, while Figure 5(b) displays the camera photograph of the DIW-printed OTFT device. The OTFT was fabricated using the Ag conductive ink, the TIPS-pentacene solution, and the PVA solution for the electrodes (i.e., source/drain and gate terminals), the OSC layer, and the dielectric layer, respectively, on Si substrate. Figure 5(c) and Figure 5(d) illustrate the chemical structures of the semiconducting material TIPS-pentacene and the dielectric material PVA, respectively.

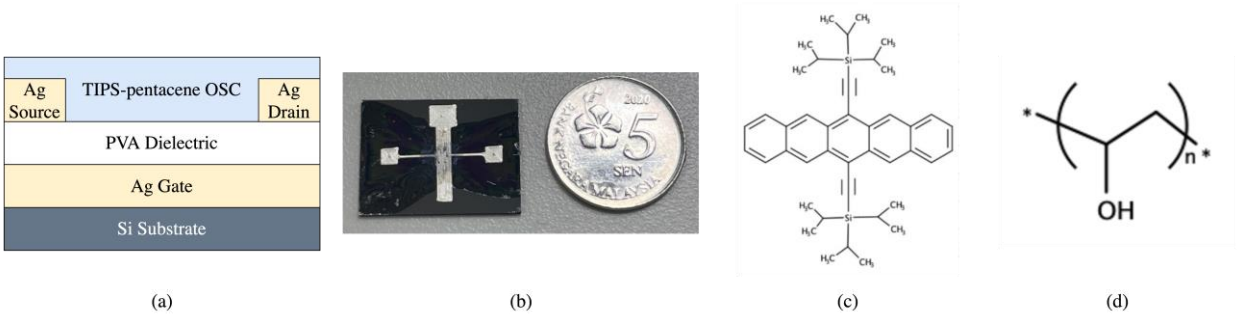

Fig. 5. (a) Schematic diagram of the device structure, (b) camera photograph of the DIW-printed OTFT device fabricated on Si substrate, (c) chemical structure of TIPS-pentacene organic semiconductor, and (d) chemical structure of PVA

The DIW-printed method has been explored to develop various sensors and other electronic circuits, as stated by Hou *et al.,* in [27]. Surprisingly, only a handful of studies have been done to employ the DIW printing technique in the deposition of the electrodes for the OTFT applications. As the channel length of the OTFT plays an important role in determining the overall performance of the OTFT, researchers usually attached additional parts to the DIW printer, such as a meniscus-guided pen, as mentioned by Kee *et al.,* in [30] in order to scale down the channel size. Figure 6(a) shows the source/drain layout of the proposed OTFT. In this work, we successfully employed the DIW printing technique to deposit the source/drain contacts with channel lengths up to micrometre size. The approximate channel length of the fabricated OTFT was 120 µm, as shown in Figure 6(b). A DIW printer deposited a relatively smooth and even pattern with an average thickness of 8.319 µm, as depicted in Figure 6(c).

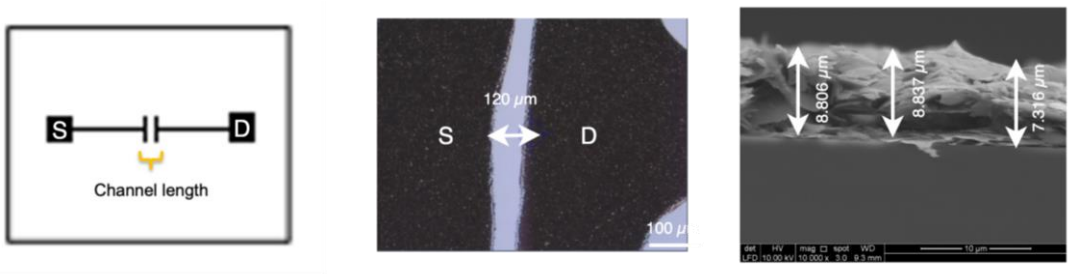

Fig. 6. (a) The layout of the source/drain contacts of the proposed OTFT, (b) LSM image of the printed channel with a channel length of 120 µm, and (c) SEM image of the printed electrode with an average thickness of 8.319 µm

As mentioned previously, the DIW printing technology has surpassed the conventional inkjet printer in terms of the selection of materials due to its compatibility with various types of inks. In this work, silver conductive ink has been used to deposit the conductive electrodes of the OTFT. No clogging issue was reported during the deposition process, and the printed patterns were deposited smoothly on the substrate, as seen in Figure 5(b). The silver conductive ink can be directly used without further modification, unlike the inkjet printing method, which needs to be tailored according to the printer's specifications.

In order to promote hole injection between the electrodes and the OSC layer, the work function of the electrode has to match the energy level of the highest occupied molecular orbital (HOMO) or the lowest unoccupied molecular orbital (LUMO) of the organic molecules as stated in [31]. In other words, a narrow energy barrier between the electrode and semiconductor is required. Figure 7 displays the energy level diagrams of the commonly used conductive inks i.e., copper (Cu), silver (Ag), and gold (Au), against the organic molecule, TIPS-pentacene and their work functions are 4.54 eV, 4.93 eV, and 5.27 eV, respectively as reported in [32,33]. Although Au's work function matches the LUMO of TIPS-pentacene the best, nevertheless, its high curing temperature (> 190 ℃) impedes its applications in flexible electronics. On the other hand, Ag shows a relatively narrow energy barrier against TIPS-pentacene with an energy gap of less than 0.4 eV and requires a sintering temperature of less than 150 ℃, making it suitable for flexible substrate applications. Hence, the Ag conductive ink was selected to deposit the electrodes in this work.

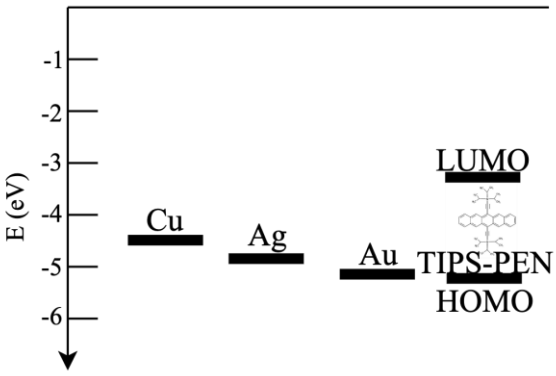

Fig. 7. Energy level diagrams of the Cu, Ag, and Au against HUMO-LUMO of TIPS-pentacene

Figure 8(a) presents an optical image of the proposed PVA-based dielectric OTFT, while Figure 8(b) portrays a water droplet contact angle on the PVA dielectric film. In general, the water contact angle describes the surface hydrophilicity. Kwon *et al.,* in their work [34] suggested that the growth of OSC film can be improved by reducing the hydrophilic and polar properties of a dielectric surface. Surface with hydrophobic characteristics shows contact angle > 90°. In this work, the D/I water droplet on the PVA surface recorded a contact angle of 64.65°, showing a slightly hydrophilic characteristic. Nevertheless, the hydrophobicity of the PVA surface can be increased by treating the surface with surface treatments. Figure 8(c) shows the SEM image of the deposited OSC layer. The spin-coated TIPS-pentacene appeared to be relatively smooth with < 40 nm thickness. It is worth mentioning that both PVA dielectric and TIPS-pentacene OSC layers were cured at temperatures between 80 ℃ to 100 ℃ to match flexible electronics requirements.

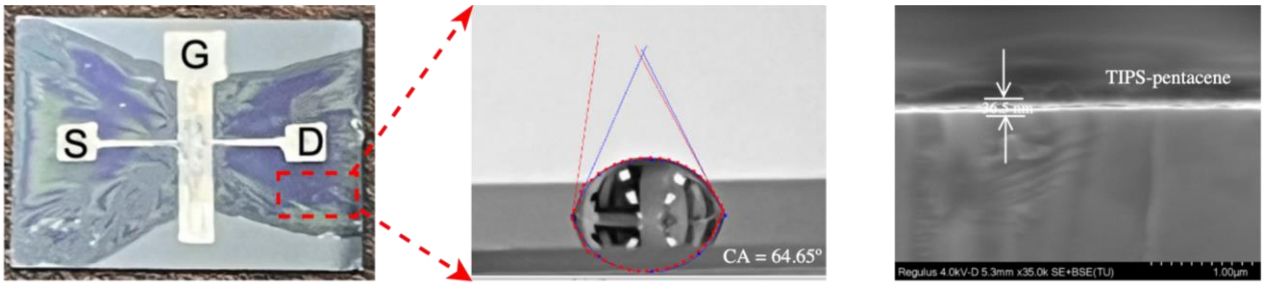

Fig. 8. (a) Optical image of the PVA-based dielectric OTFT, b) D/I water droplet on the PVA surface with 64.65° contact angle, and (c) SEM image of the TIPS-pentacene layer with 36.5 nm thickness

3.2 Electrical Characterization of the OTFT

Next, the electrical characteristics of the OTFT were evaluated. Figure 9(a) shows the output characteristics (I_{DS}-V_{DS}), while Figure 9(b) and (c) display the transfer characteristics ($|I_{DS}|$-V_{GS}) of the proposed BGBC OTFT and its corresponding square-root I_{DS} ($\sqrt{I_{DS}}$-V_{GS}) curve, respectively. V_{DS} was varied from 0 to -3 V with -0.1 V interval at different V_{GS} ranging from 0 to -10 V. Negative voltages have been applied since holes are the majority charge carriers in TIPS-pentacene. From Figure 9, it can be seen that the proposed TIPS-pentacene OTFT exhibited a typical p-type field effect transistor behaviour. Distinct linear and saturation regions can be observed from the output curves, as depicted in Figure 9(a). From the transfer curve and its corresponding square-root I_{DS} curve in Figure 9(b) and (c), the saturation mobility μ_{sat} of about 4.49×10^{-1} cm^2/Vs, the threshold voltage V_{th} of -1.5 V, and the on/off current ratio (I_{ON}/I_{OFF}) up to 10^8 (V_{GS} = -4 V and V_{DS} = -1.5 V) were extracted. The field effect mobility of the OTFT at saturation region was calculated using Eq. (2) as done in [35]

$$\mu_{sat} = \frac{L}{W}\frac{1}{C_i}\frac{\delta^2 I_{DS}}{\delta V_{GS}{}^2} \tag{2}$$

Where μ_{sat} is the saturation mobility, C_i is the geometric capacitance of the dielectric, while L and W are the channel length and width, respectively. The deposited OSC layer plays an important role in determining the mobility of the OTFT. In this work, the fabricated OTFT shows a fair μ_{sat} as compared to the other inkjet-printed OTFTs, as recorded in Table 1.

Besides that, a subthreshold swing S is used to determine whether a good interface is formed between the dielectric and the OSC layers. The S value was calculated from the inverse of the subthreshold slope and can be expressed as in Eq. (3) as done in [36]. Apart from that, the S can also be written as Eq. (4) and can be used to calculate the lowest theoretical S at room temperature.

$$S = \frac{dV_{GS}}{d(log I_{DS})} \tag{3}$$

$$S = \frac{K_B T}{q} ln10 \tag{4}$$

Where T is the temperature in Kelvin, K_B is Botlzmann's constant, and q is the elementary charge. At a room temperature of 300 K, S is determined to be 57 mV/decade. Remarkably, the proposed OTFT achieved a subthreshold swing S of 66.8 mV/decade, nearly reaching the theoretical limit at room temperature. This confirms a good interface between the PVA dielectric and TIPS-pentacene layers due to low deep gap states localized near these two layers' interface.

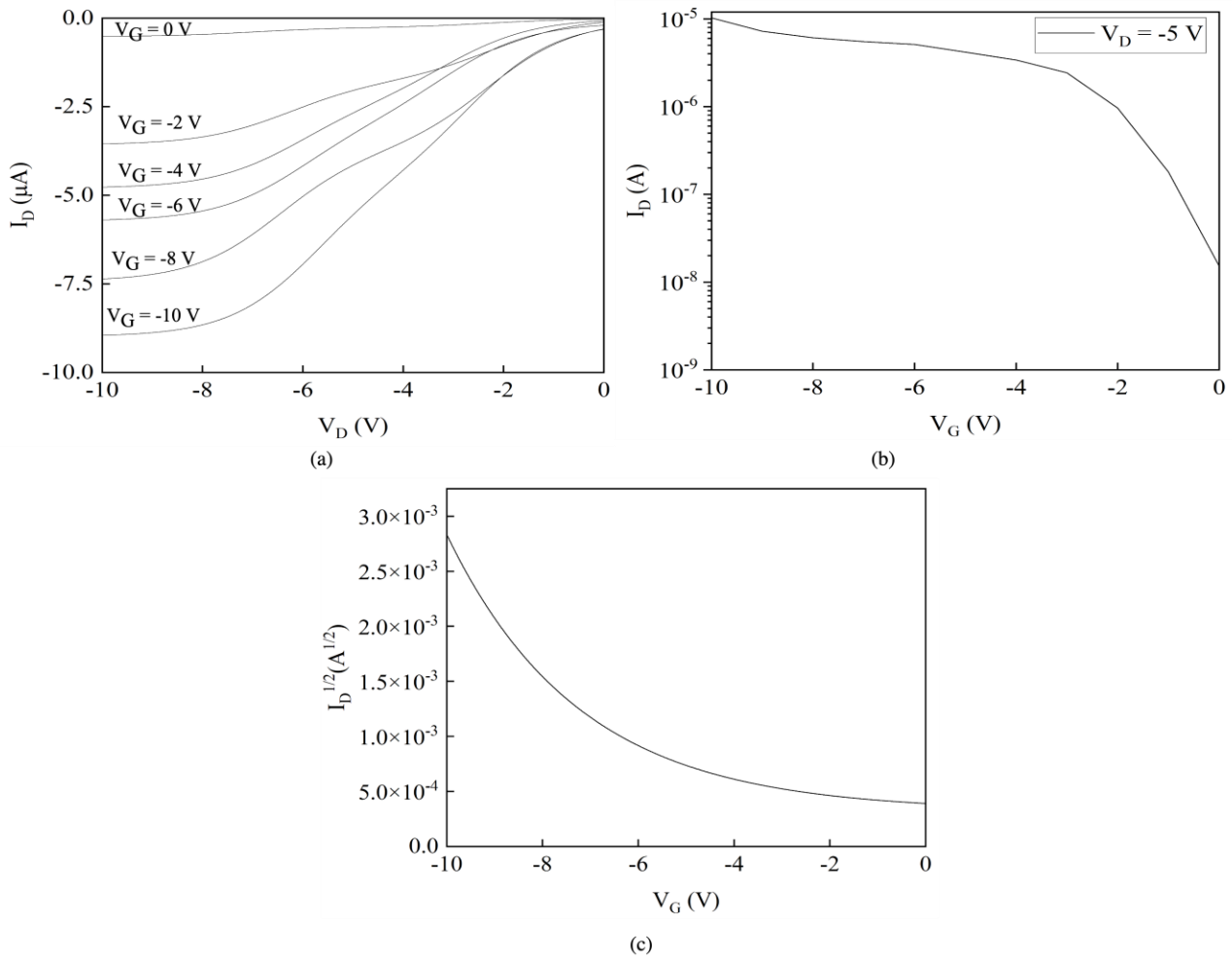

Fig. 9. Characteristics of BGBC OTFT: (a) Output (I_{DS}-V_{DS}), (b) transfer ($|I_{DS}|$-V_{GS}) characteristics, and (c) square-root I_{DS} ($\sqrt{I_{DS}}$-V_{GS}) curve of the proposed all-solution processable OTFT based on TIPS-pentacene OSC layer and high-*k* PVA dielectric layer

On top of that, in this study, we successfully fabricated the OTFT with a low operating voltage using a high-*k* dielectric material. A major improvement in terms of the operating voltage can be seen as compared to previous work by Yusof *et al.,* in [29]. Previously, the operating voltage of the OTFT reached up to -60 V. In this work, the low-voltage OTFT was realized by using a polymeric PVA dielectric layer. The proposed OTFT can function at the operating voltages < -15 V. The high-*k* material has been proven to increase the overall gate capacitance, which, in return, improves the operating voltage of the device. Besides, high I_{ON}/I_{OFF} is achieved due to high drain current during on stage with minimum leakage current during off state. This may be attributed to the fair quality of deposited semiconductor and dielectric layers, as shown in Figure 8.

In general, the overall performance of the fabricated device is comparable with that of those fabricated using an inkjet printing technique, as listed in Table 1. Based on Table 1, the proposed OTFT not only demonstrated a low-operating voltage as well as low V_{th}, but also showed up to two order enhancement in terms of I_{ON}/I_{OFF}. Besides, the μ_{sat} achieved is on par with the other devices as well. In fact, the proposed DIW-printed OTFT shows an equivalent performance as thermally evaporated OTFT, as shown by Mahato *et al.,* in [37]. In a nutshell, based on the results summarized in Table 1, it can be verified that the proposed DIW printing technique can be exploited to fabricate the OTFT without compromising its electrical and morphological performances, while the high-*k* dielectric layer successfully reduced the operating voltage of the proposed device. Interestingly, the

DIW printer can be used to deposit the source/drain electrodes up to micrometre channel length without clogging issues due to its compatibility with various materials, including high-viscosity inks. This makes the DIW technology more flexible and can be further explored to fabricate low-voltage OTFTs in novel flexible electronic circuits and sensors.

Table 1
Comparison of the proposed OTFT performance with other state-of-the-art works

Reference	[29]	[36]	[37]	[38]	[39]	This work
S/D Deposition Technique	DIW-printed	Inkjet-printed	Thermally evaporated	Inkjet-printed	Inkjet-printed	DIW-printed
OSC Layer	TIPS-pentacene	F8T2	TIPS-pentacene	FS0027	TIPS-pentacene	TIPS-pentacene
Dielectric Layer	SiO_2	Cytop®	PVA	PVP	PVP	PVA
Saturation Mobility μ_{sat} (cm^2/Vs)	4.28×10^{-5}	9.70×10^{-3}	3.4×10^{-2}	1.90×10^{-4}	6.50×10^{-2}	4.49×10^{-1}
Threshold Voltage V_{th} (V)	-0.40	-12.50	-13.8	-0.90	1.24	-1.5
On/Off Current Ratio I_{ON}/I_{OFF}	10^2	10^2	10^3	10^2	10^3	10^8
Subthreshold Swing SS (mV/decade)	10	378	4200	-	-	66.8

4. Conclusions

Recent developments in DIW printing technology have broadened its applications in flexible electronics. The ability to rapidly pattern functional materials over a broad range of materials without clogging issues has made this technology a better option than the inkjet printing technique for OTFT fabrication. Besides, the high operating voltage of the OTFT impedes its implementation in real-life applications. Hence, in this work, we successfully developed a solution-processable OTFT with channel length up to a micrometre scale using a DIW printing method. On top of that, the utilization of a high-*k* PVA material as the dielectric layer allows the realization of the OTFT working at a low operating voltage of less than -15 V. Remarkably, the proposed BGBC TIPS-pentacene OTFT exhibited saturation mobility of 4.49×10^{-1} cm^2/Vs, a threshold voltage of -1.5 V, an on/off current ratio of 10^8, and a subthreshold swing up to 66.8 mV/decade. Besides, the overall processing temperature was kept below 150 ℃ to suit flexible electronics requirements. Thus, we believe that continuous efforts in scaling down the channel length by using the DIW printing technique and utilizing a high-*k* material for the dielectric layer can further improve the overall operation of the OTFT. This will eventually lead to the next generation of highly embedded electronics at low cost and low operating voltage for flexible devices and wearable systems.

Acknowledgement
This research was funded by the Ministry Of Higher Education Malaysia for the Fundamental Research Grant Scheme with Project code: FRGS/1/2020/TK0/USM/02/30. The authors also would like to express gratitude to USM School of Electrical and Electronic Engineering Semiconductor Lab (SEEE Semiconductor Lab) for the research facilities to conduct the research.

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