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Prototype of Water Dam System by Using FPGA Platform

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ABSTRACT

A water dam system is a promising system which uses the aid of sensor to detect the real time depth of stream by measuring the height of the buoyant floating on the water. The goal of this project is to design a robotic water dam system which can raise its floodgate or gate after receiving the commands from user. It is designed to detect the water level and notify the user immediately with the aid of notification system hence user could command to raise or close the floodgate. The paper demonstrates a prototype of a working and operational water dam system by means of FPGA platform and its procedures.

1. Introduction

Dam or water dam is a huge structure which can be found across a river to store water. Tosun H. in his works described dam has several crucial functions as it provides water for human consumption and also industrial processes [1]. Apart from being used for retaining water as reservoir, dam can serve as generator to generate hydroelectric power. Besides, it can function as floodgate to reduce peak discharge of floodwater due to thunder storm or heavy snow and increase the depth of river water to allow navigation of ships and cruises [2]. A multipurpose dam could contribute in recreational activities such as swimming, fishing, and so on.

The dam has many features and one of them is movable gates and valve to control the release of surplus water downstream [3]. This feature has the capability to transfer or deliver water to a power station which located far away through designed canals. Other auxiliary works are systems which function to evacuate or flush out silt which accumulated in reservoir, permit the passage of ships through the dam site and some devices which assist in fishing.

In the experiments conducted in Brown and Burke, dam is sometimes known as central structure in a multipurpose scheme designed to conserve water [4,5]. In developing countries, a multipurpose dam holds an important role as it brings significant benefits related to hydroelectric production, agricultural development and also industrial growth. However, dam has the probability to become one of the environmental concern due to their impact on migrating fish and riparian ecosystem. Moreover, large reservoirs able to inundate vast tracts of land which used to be home of many and

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this has caused an opposition to dam by questioning whether the benefits of dam projects worth the costs of the projects.

In terms of electronic device used for the project, an integrated circuit called field-programmable gate array (FPGA) utilised for programming to the required functionality of specific applications. By using the prebuilt logic block and programmable routing resources, the custom hardware functionality can be implemented without using a breadboard or soldering iron [6]. The procedure had been explained in [7], however, the FPGA configuration generally is specified by using a Hardware Description Language (HDL) which is quite related to that used for an Application-Specific Integrated Circuit (ASIC). One of the benefits of FPGA is it contains an array of programmable logic blocks and a hierarchy of reconfigurable interconnects that allow the blocks to be wired together which can be seen in many logic gates that can be inter-wired in varied configurations [8]. Combinational functions or simple logic gates could be configured to perform in FPGA with the comprehensive explanation in [9]. Most of the FPGA could be reprogrammed to run varied logic functions with the aid of memory elements such as simple flip-flops, also it allows flexible reconfigurable computing as performed in computer software. Grout I. explains sequential logic circuit based on combination logic elements (latches and flip-flops that will be grouped together to form register) [10] and control strategy implementation such as PID [11] could be the better choice for lower demand for computation resource.

2. Project Description

The mechanical system and dam operation involve in designing a digital circuit by means of Altera Quartus II 13.0 Web Edition with combining analogue circuit to function the overall dam system.

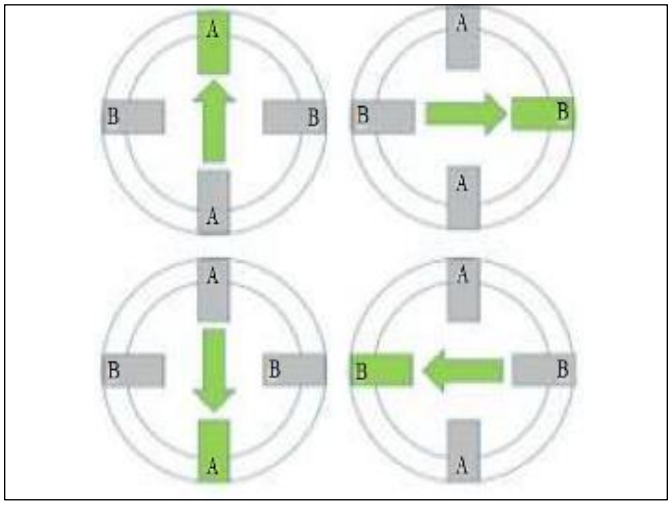


Fig. 1. Full Step (Low Torque) with one phase HIGH

Two stepper motors are used to produce preferred outputs and FPGA board to generate outputs for IC ULN2003 in which to initiate motor driver for 35BY48L-97 stepper motor. Diagram illustrate in Fig. 1 is the effect of sequence on rotational motion of the stepper motor applied which known as full step (low torque) with one phase HIGH.

Table 1
Stepper Motor Steps and Inputs for 45 Degree Rotation

Step	Input			
	A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0

The decision to design the stepper motor rotate in full step (low torque) with one phase HIGH motion as instructed in learning system procedure [12]. The step angle of the stepper motor is set 7.5 degree per step, therefore to make it moves 6 steps per click so that it could rotate 45 degree per click and raise the gate 25% from its max opening of the gate. The reason is to have a better control of the output of stepper motor. Assuming that the input pins controlling the 4 phases of stepper motor be A, B, C and D. The input for each phase is shown in Table 1 to ensure the motors move as preference.

A clock pulses generator is designed to produce 6 clock pulses by pressing input key once. The output of the clock pulses generator connected to the clock of the modified bidirectional ring counter and shift register to provide outputs for IC ULN2003 motor driver so that it could change its state for 6 times. Furthermore, a frequency divider is designed to reduce the high built in 50MHz frequency of the FPGA board to preferred range which is 3Hz to 6Hz.

In addition, several features are included in circuit to ensure the circuit is functioning as expected and IR sensors are included to detect the buoyant in stream water to estimate the current depth of the stream. A security lock system is also included in the circuit to ensure the system is in the right hand. A display system is attached to indicate user the dam gate's status. Lastly, a modified bidirectional ring counter and shift register are designed to assist bidirectional rotation of stepper motor. The features of the project are shown in Table 2.

Table 2
Features of the Water Dam System

Features	Functions
Stepper motor analogue circuit	To amplify the output from GPIO pin of FPGA to power the stepper motor through motor driver IC ULN2003
Clock pulses generator	To produce 6 clock pulses at one click
Modified Bidirectional Shift Register and Ring Counter	To provide bidirectional rotation in stepper motor
Frequency divider	To divide the high 50MHz built in frequency of the FPGA board
Display system	To display the dam gate's status
Notification system	To notify user the depth of water with the aid of IR sensor
Security lock system	To secure the dam and ensure it is in the right hand

3. Methodology

3.1 IR Receiver and Overall Digital Schematic Circuit

In the case of the IR receiver does not receive a signal, the potential at the inverting input goes higher than that non-inverting input of the comparator IC (LM339). Thus, the output of the comparator goes low, but the LED does not glow. On another case of the IR receiver module receives

signal to the potential at the inverting input goes low resulting the output of the comparator (LM 339) goes high and the LED starts glowing. Therefore, resistors denoted as R1 (100), R2 (10k) and R3 (330) are used to ensure that minimum 10 mA current passes through the IR LED Devices like Photodiode and normal LEDs respectively. Resistor VR2 (pre-set=5k) is used to adjust the output terminals. Resistor VR1 (pre-set=10k) is used to set the sensitivity of the circuit Diagram.

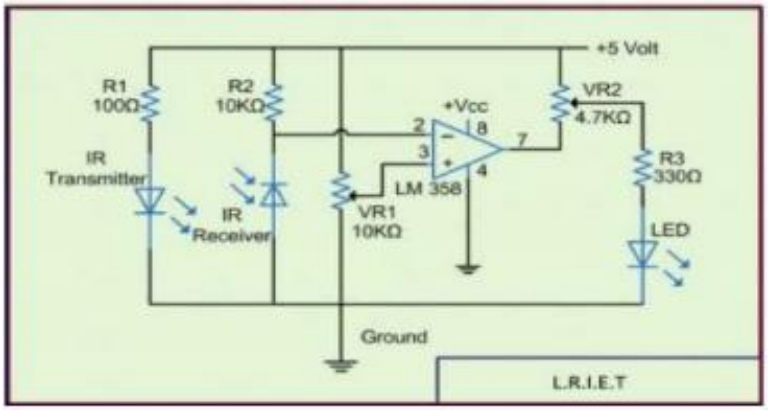


Fig. 2. IR Sensor circuit

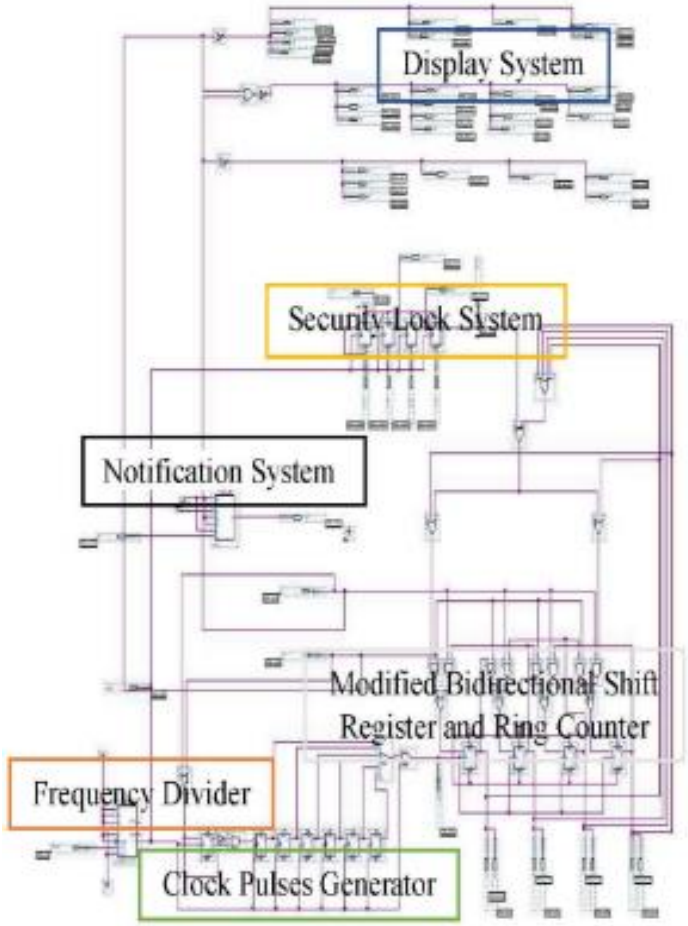


Fig. 3. Digital Schematic Circuit of the Water Dam System

The digital schematic circuit of the Water Dam System is designed through combination of several systems. The systems include Display System, Notification System, Security Lock System, Frequency Divider, Clock Pulses Generator and Modified Bidirectional Shift Register and Ring Counter.

3.2 Notification System

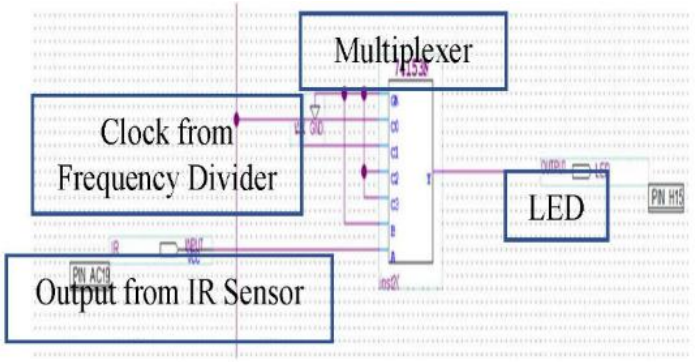


Fig. 4. Digital schematic diagram for Notification System of the Water Dam System

The digital schematic diagram for Notification System as shown in Fig. 4. An IR sensor is used to detect the buoyant place in the stream as the buoyant will indicate the depth of the stream or river. When water depth increases and surpasses certain height and the IR sensor will be triggered and become HIGH, as it becomes HIGH the input in S1 and S0 in the multiplexer will 0 and 1, respectively. Hence, the output will display the input from C1 which HIGH and the LED is will light continuously.

Vice versa, if the IR sensor output is LOW, the output LED will display the input from C0 which the clock of the overall system and the LED is will keep on blinking indicating the system is still in function.

3.3 Security Lock System

The output will only be HIGH if the user has entered the correct password and the water dam system could only function when the output from the security lock system is HIGH, else the dam will not be able to function. When all of the CLEARs are activated indicating that the passwords entered are incorrect and the system will stop functioning.

Inversely, if the passwords entered are correct the CLEARs will be deactivated, and the output will become HIGH. The LEDs from each D flip-flop will become HIGH and light up when the password entered is correct. However, after the correct passwords are entered the user is not allowed to change the pin of the passwords.

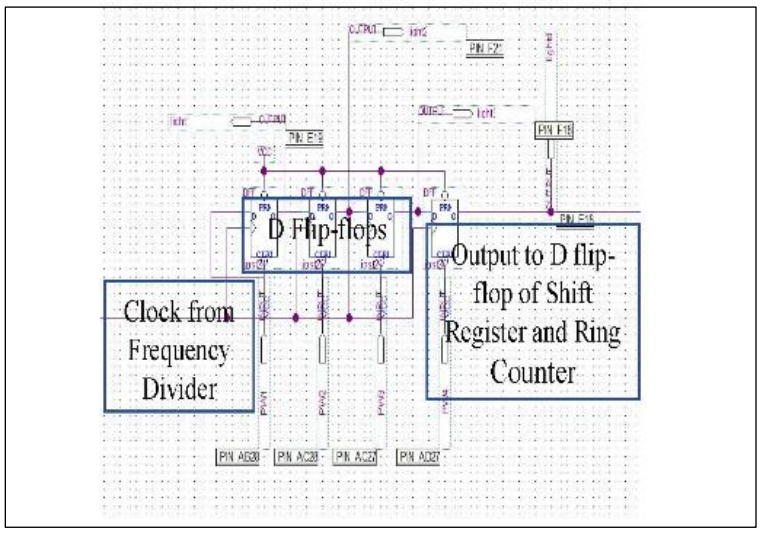


Fig. 5. Digital schematic diagram for Security Lock System

3.4 Frequency Divider

The default frequency from the FPGA board used in the system is 50MHz which is significantly high for stepper motors used in the system. Therefore, an IC 74292 is used to reduce the frequency so that the stepper motor could work. Table 3 shows the function table for IC 74292.

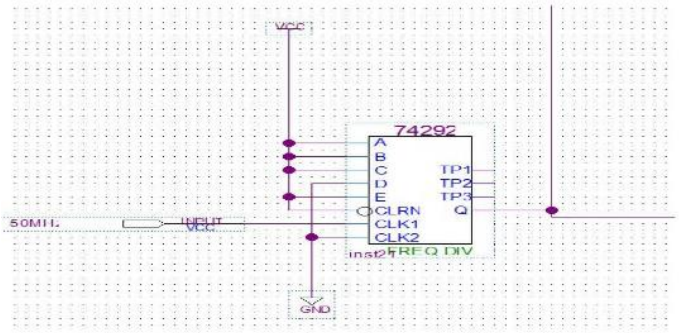


Fig. 6. Digital schematic diagram for Frequency Divider

Table 3
Function Table of IC 74292

H	L	H	H	L	2^{22}	4194304
H	L	H	H	H	2^{23}	8388608
H	H	L	L	L	2^{24}	16777216

The connection of IC 74292 in Table 3 is 'HLHHH'. Hence, according to the table we can conclude that the frequency is divided by 223 and the output of the frequency after going through IC 74292 is:

$$Clock\ frequency = \frac{50M}{2^{23}} Hz \approx 5.96Hz \quad (1)$$

As a result, the final clock frequency is reduced to approximately 5.96Hz which is suitable for the operation of stepper motor.

3.5 Clock Pulses Generator

Clock Pulses Generator functions to generate 6 clock pulses to generate 6 clock pulses for the Modified Bidirectional Shift Register and Ring Counter so that it could shift 6 times. The stepper motors used in the system able to move 7.5 degree per step. Therefore, 6 clock pulses are needed to move 45 degree per shifting which is equivalent to the 25% of the max opening.

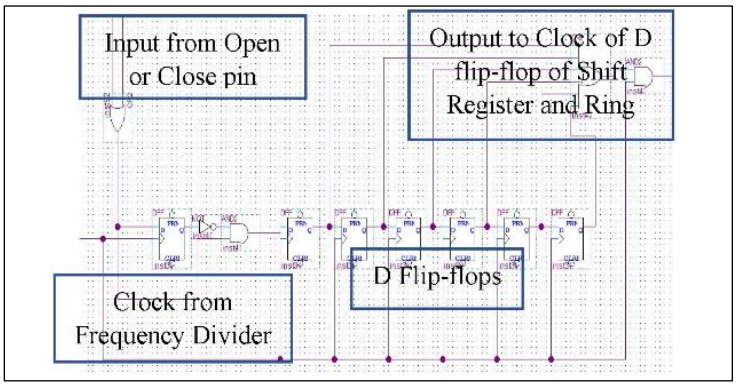


Fig. 7. Digital schematic diagram for Clock Pulses Generator

The inputs of the first of the six flip-flops is connected to an AND gate. The inputs of the AND gate are from the inverted output of the one D flip-flop on the left and the inputs of the Open and Close pins.

All of the clocks from the system are connected to the same clock generated by the Frequency Divider. Open and Close status are the inputs of the OR gate in the system in the case of either inputs of Open or Close is HIGH for once, the Clock Pulses Generator will generate 6 clock pulses for the system.

Initially, the output of the D flip-flop on the left is LOW and is inverted to become HIGH at the input of the AND gate. The moment Open or Close pin is triggered the output of the D flip-flop on the left become LOW while the previous output of the D flip-flop which is HIGH combine with the HIGH from the OPEN or CLOSE inputs and caused the output of the AND gate become HIGH. As a result, the 6 D flip-flops start to produce HIGH at output. Immediately after the first HIGH output of the AND gate, the next output be LOW as there's an Inverter in between AND gate and D flip-flop on the left.

The output of the first D flip-flop on the right will be HIGH as the input is HIGH. Subsequently, the second to sixth D flip-flop will also generate HIGH output as the inputs are also HIGH. Hence, this result in the output of the 6-Inputs OR gate to be HIGH for a period of 6 clock pulses.

3.6 Modified Bidirectional Shift Register and Ring Counter

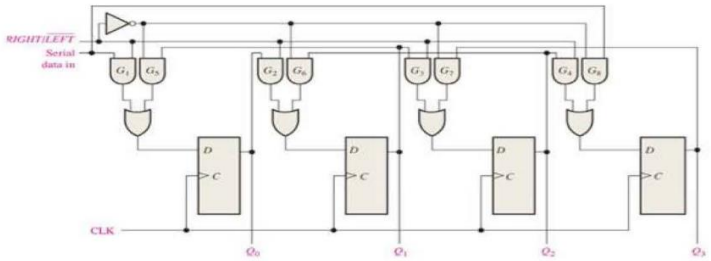


Fig. 8: Bidirectional shift register schematic

Function of G1 is for shift right serial data entry while G8 is for shift left serial data entry. According to the schematic, when RIGHT/LEFT is HIGH it will enable G1 for serial data entry and causing G1 to G4 to shift data to right at every clock pulse. Inversely, when RIGHT/LEFT is LOW it enables G8 for serial data entry and causing G5 to G8 to shift data to left at every clock pulse.

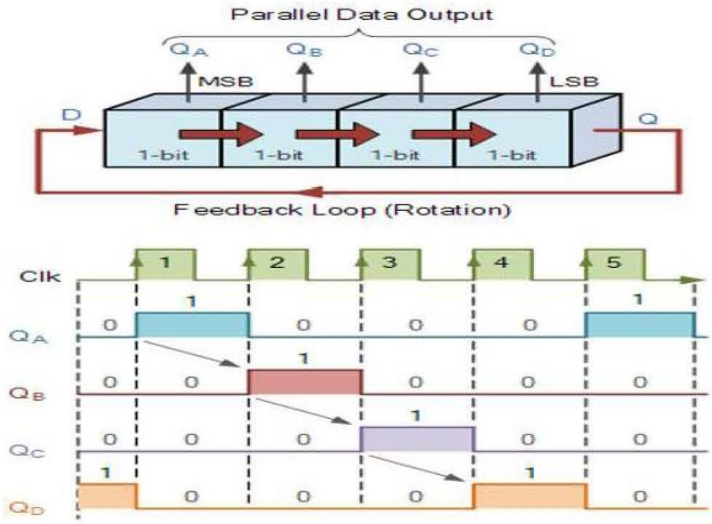


Fig. 9. Ring Counter's Feedback Loop and its shifting pattern

Function of a ring counter is to loop the last output generated by the last flip-flop and make it become the next input for the first flip-flop as shown in Figure 9.

Bidirectional Shift Register and Ring Counter is modified from both bidirectional shift register and ring counter. In short, it comprises of the properties of a ring counter as well as bidirectional shift register. The combination of both shift register and ring counter will result in data not only able to move forward or backward, moreover it could loop the last output from the last flip-flop and make it the input of the first flip-flop.

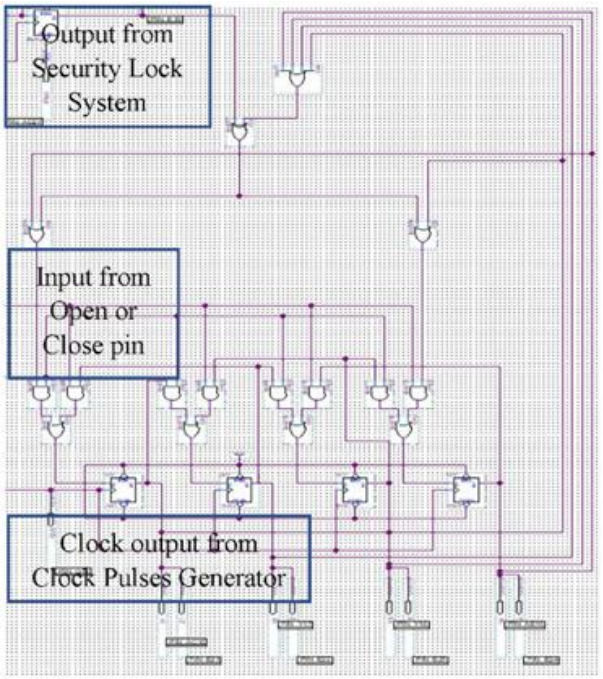


Fig. 10. Digital schematic diagram for Modified Bidirectional Shift Register and Ring Counter

All clocks of the 4 D flip-flops in Modified Bidirectional Shift Register and Ring Counter are connected to the clock output from Clock Pulses Generator so that the flip-flops could receive only 6 clock pulses (refer Figure 10). The generated clock pulses ensure that the stepper motors shift data

for only 6 times so that preferred rotation of 45 degree could be achieved. The inputs from Open or Close pin acts as RIGHT/LEFT in shift register which function to change the direction of data input either from left to right or right to left.

While for the upper part of the circuit, the one of the input XOR gate is connected to the output of the Security Lock System to provide an initial HIGH signal after correct passwords are entered while the 4-inputs OR gate provides LOW signal as the initial output of the flip-flops are LOW. As a result, a '1' looped in the ring counter as the XOR gate provides HIGH signal. After that, the XOR prevents the HIGH signal from the Security lock system from causing malfunction in the shift register as the 4-inputs OR provides a HIGH signal. Then, the first loop LOW output will be resulted in XOR gate due to both inputs of XOR gate are HIGH from Security Lock System and HIGH from 4-inputs OR gate. While the 2 OR2 gate will allow the data to loop and shift like a ring counter.

3.*7 Notification System*

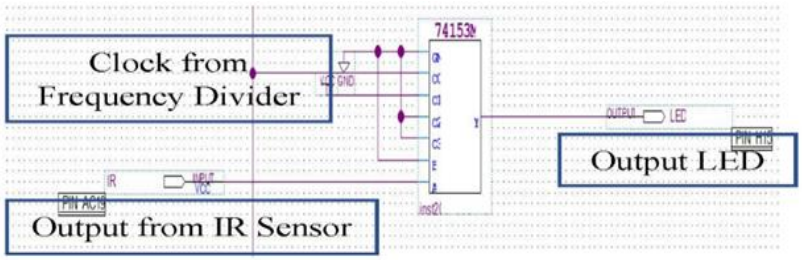


Fig. 11. Digital schematic diagram for Notification System

A multiplexer is used in this system in order to select preferred output. When the water level detects an increasing level of water, the IR sensor will produce HIGH output and cause the multiplexer to generate output from C1 as S1 and S0 is '0' and '1' respectively. Or else, if the IR sensor produce a LOW output it will cause the multiplexer to generate output of C0 which will results in blinking of LED which indicating the Water Dam System is working well. The output C0 is generated because S1 and S0 is '0' and '0' respectively.

3.8 Display System

From the digital circuit designed in Fig. 12, the seven segment display is designed to display the words 'CLOSE' and 'OPEN' when user's command is received. Seven segment display for FPGA board is active-LOW, hence three NOT gates is placed in order to activate the segments display system.

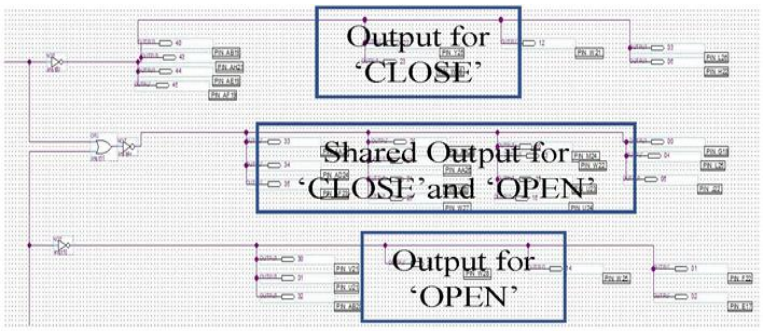


Fig. 12. Digital schematic diagram for Display System

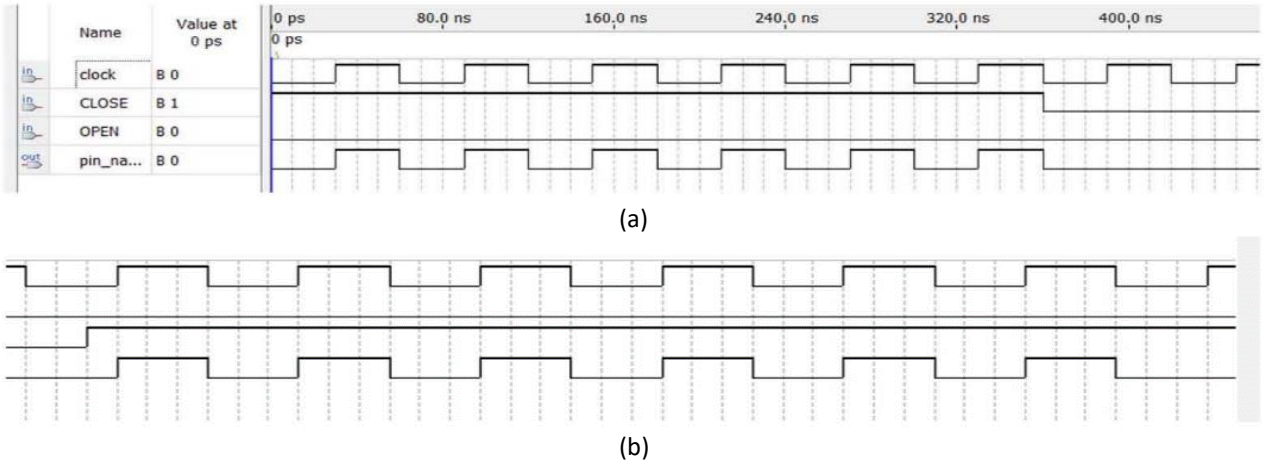
4. Hardware and Circuit Construction

The water dam system consists of several major components of completing system. Based on the Figure 13, it requires the correct passwords, operations buttons commanded by user and also indication from IR sensor to allow the stepper motor to rotate which indicating the open and close of the floodgate. The opening and closing of the floodgate will open or close at 25% of its maximum opening and closing once 'OPEN' or 'CLOSE' is triggered.

Fig. 13. Block diagram architecture of Water Dam System

5. Results and Simulations

5.1 Clock Pulses Generator



(a)

(b)

Fig. 14. Simulation waveform of clock pulses generator when (a) 'CLOSE' is triggered (b) 'OPEN' is triggered

The simulation showed the clock pulses generator produces six pulses or clocks for the Modified Bidirectional Shift Register and Ring Counter so that the stepper motors can be rotated 45 degree in which equivalent to 25% of the max opening of the gate.

5.2 Security Lock System

From the Figure 15(a) and 15(b), one could see that when the passwords entered are incorrect the final output will be LOW; otherwise the correct passwords are entered the final output will be HIGH and the water dam will start to function.

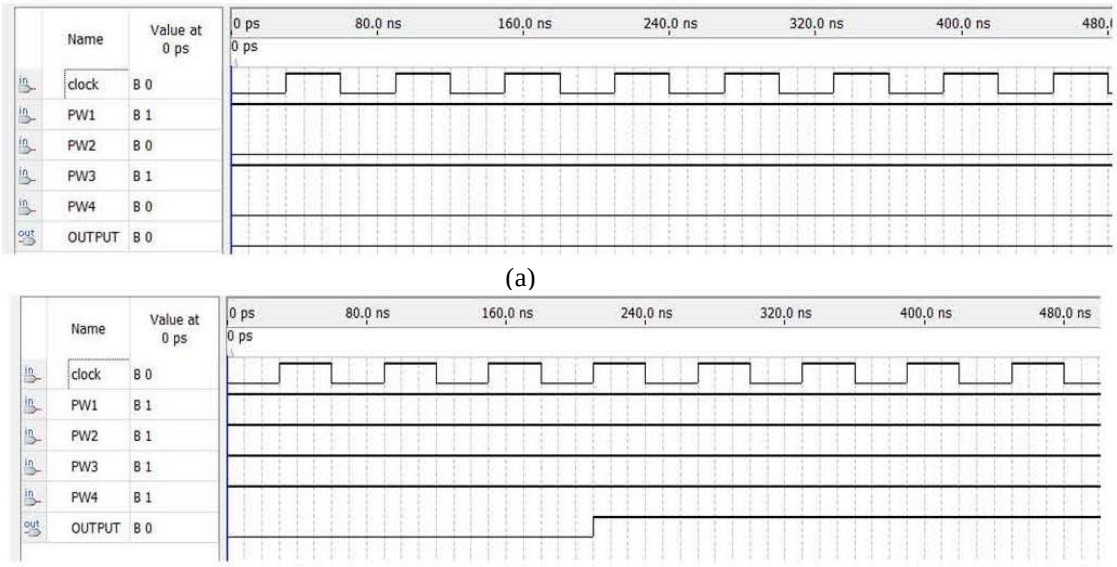


Fig. 15. Simulation waveform of Security Lock System when passwords entered are (a) incorrect (b) correct

5.3 Security Lock System

Figure 16 showed that in the situation of the IR sensor is LOW the output Led only blinks indicating the system is functioning. When the IR sensor detected high water level it will become HIGH and cause the output LED to light to notify user.

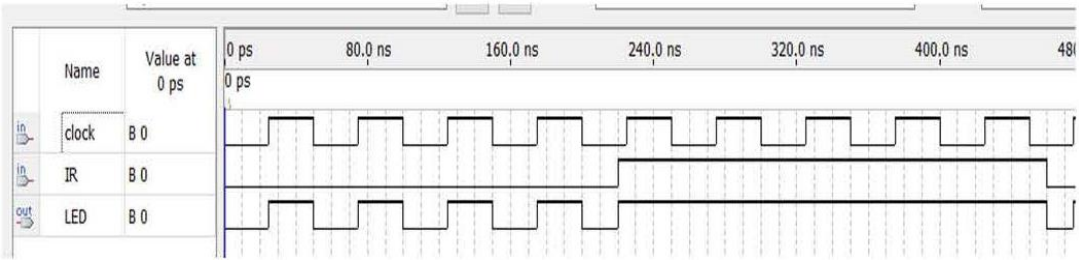


Fig. 16. Simulation waveform of Notification System

5.4 Modified Bidirectional Shift Register and Ring Counter

From the Figure 17(a) and 17(b), the system has bidirectional property to allow the stepper motor to rotate in clockwise or anti-clockwise direction as the '1' shifted from left to right in 'CLOSE' while in shifted inversely in 'OPEN'.

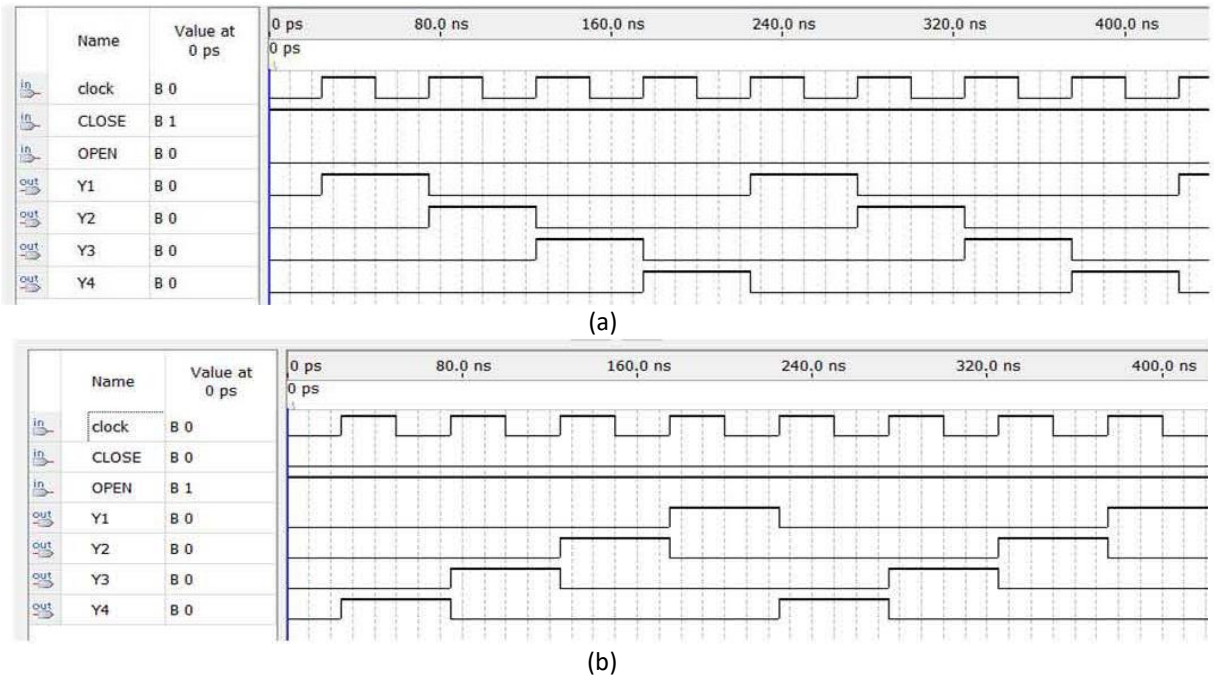


Fig. 17. Simulation waveform of Modified Bidirectional Shift Register and Ring Counter when (a) 'CLOSE' is triggered (b) 'OPEN' is triggered

6. Conclusions

In conclusion, by applying Full Step (Low Torque) with one phase HIGH which is shown in the Section 2 and 3. Full step mode or usually know as low torque mode. In this mode the motor is operated with only one phase (group of windings) energized at a time. This mode requires the least amount of power from the driver of any of the excitation modes. The implementation a variety of systems in order to complete the project is successful met the objectives. The systems included are Display System, Notification System, Security Lock System, Frequency Divider, Clock Pulses Generator and Modified Bidirectional Shift Register and Ring Counter. Each system and features has specific function which makes the Water Dam System complete.

The mechanical part through the idea of pulley system where there are strings attach to the stepper motors and the floodgate. This enable user to raise or close the gate as user preference. The floodgate will raise or close up to 25% of its max opening once a "CLOSE' or 'OPEN' is triggered. The Notification System will also notify the user once the water level is high or low so that user could decide whether to raise or close the floodgate. Besides, for security purpose, a Security Lock System is included to ensure the Water Dam is in safe hand. However, there are some improvement could be made as we could use more components such as buzzer to strengthen the Notification System.

Acknowledgement

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