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# Electronic Mailbox Designed with FPGA Platform

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**ABSTRACT**

An electronic mailbox is a device proposed to detect letter delivered by post-man when the mailbox is opened or closed to notify the user for their new mail. The goal of this work is to make a mailbox model that can calculate the amount of mailbox opened by postman and lights up the yellow or red LED and buzz the buzzer to indicate an existing mail inside the mailbox. It is de-sign to demonstrate the feasibility of using a Field Programmable Gate Array (FPGA) to implement custom hardware functionality. The present hardware consists of an infrared sensor (IR), a buzzer, seven segment display, FPGA and pushbuttons. This research paper demonstrates our proposed ideas, de-scribes the design of a smart mailbox, the prototype, and the current results of work.

## 1. Introduction

Nowadays, the world is full of science and technology, they replace traditional items in many ways and fields. One of the most significant change is the propose of Electronic Mail (e-mail). Nightingale *et al.,* [6] discussed two types of communication within companies be means of classical communication and modern communication. Shahriari *et al.,* [7] emphasized of the transformation in business communication that email has become an indispensable part of daily business activities in nearly all aspects of commerce. The massive breadth of populations using email regularly can be attributed, in large part, to its accessibility and general usefulness. However, traditional letter still stands in today's world, as people take paper letter as a more persuasive evidence compared to e-mail as was described by Leonardi *et al.,* [4]. For example, government letters, credit card bills, electricity and water bills, business letter, and offer letters. You will never want to miss any of these because it may cost you a lot. Moreover, residents who have their mailbox that is pretty far from their front door especially those who stay in an apartment or a village, they frequently have to walk out and check to see if there has been a new mail delivered or sometimes they might forget to check their mail.

Therefore, a mailbox that can notify the user of their new mail as solutions are being worked out. Researchers [2,8] have developed mailbox integrated with GSM to notify the receipts on the incoming mail. This smart mailbox is a way to help notify the user to collect their mail on time to avoid them forgot to collect it especially when important letter was delivered as it will outcome a

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problem to them. FPGA based system is chosen to programme this work as it is very flexible, reusable, and quicker to acquire. Field-programmable gate array, also known as FPGA, is a semiconductor device that can be programmed and reprogrammed to perform desired function or application after manufacturing. The detail of steps and procedure have explained in Altera, 2013. It contains an array of configurable logic blocks that is connected via reprogrammable interconnects. The book by Ndjountche [5] explains that the logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In this work, the FPGA board used is Altera DE2-115.

An infrared sensor is an electronic device, that emits in order to sense some aspects of the surroundings. An IR sensor can measure the heat of an object as well as detects the motion. Zappi *et al.,* [9] mentioned that these types of sensors that measure only infrared radiation rather than emitting it is called as a passive IR sensor. Usually in the infrared spectrum, all the objects radiate some form of thermal radiations. These types of radiations are invisible to our eyes, that can be detected by an infrared sensor. The emitter is simply an IR LED (Light Emitting Diode) and the detector is simply an IR photodiode which is sensitive to IR light of the same wavelength as that emitted by the IR LED. When IR light falls on the photodiode, the resistances and these output voltages, change in proportion to the magnitude of the IR light received.

## 2. Project Description

The purpose of this work is to build and construct a circuit with combination of digital and analog that take in inputs from humans' action towards the mail-box and output the conditions inside the mailbox to the host as a notification. This work is fully programmed through FPGA by using QUARTUS II 9.1 Web Edition. Block Diagram is used to programme the FPGA, mostly on digital part of the circuit.

The overall concept of this work is the mailbox will display the number of mailboxes opened by postman, so the user knows how many times the postman have come to deliver their mail and collect it before the number will keep increasing. The up counter in FPGA is designed to count the number of mailboxes opened or closed by the postman for seven time and stops afterward until the user collect all their mail and push the reset button by closing the backside of the mailbox and the counter start count from zero. The IR sensor detect the letter inside the mailbox and it will output a signal to yellow LED. The yellow LED lights up and the buzzer in the user house buzzes to notify them to collect their mail immediately. If they still not collect their mail until the number display show seven, the yellow and red LED will light up to give a warning to users for their uncollected mail.

The mailbox's body designed is a cuboid equipped with two doors which located at the both front and back of the body. Both doors with the hinge at the bottom which makes the door can be opened vertically downward and be closed vertically upward.

There is a 3cm x 3cm cut-through square at the bottom of the body in order to attach the IR sensor with the receiver facing into the mailbox.

Two thin pieces of magnet bar are pasted at the upper part of the door and the wall which will be in contact with the door when the door closed, same goes to the second door. The location of the magnet bar has to be very accurate so that two magnet bars will attract each other.

Two pushbuttons are attached to the upper part of the inner wall of mailbox's body with the pressable part facing out and the bottom part of the pressable part parallel with the outer vertical wall. This arrangement enables the pushbutton to be pressed when the door closed and depressed when the door opened. The pushbutton attached to the front door is called by front pushbutton and the one attached to the back door is called by back pushbutton.

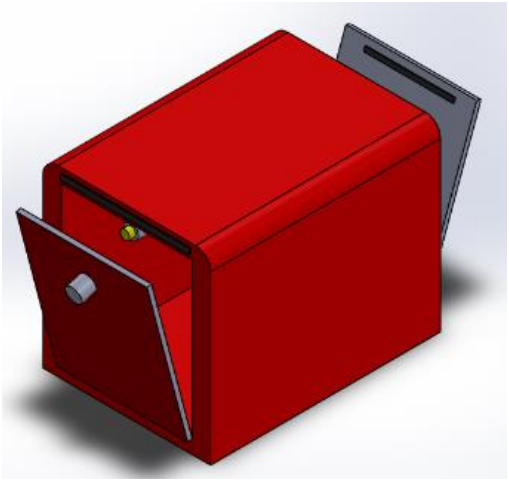

**Fig. 1.** Idea of Mailbox Body

## 3. Programming of FPGA Board

The first work is taking instructions and advise given in Cofer [3] in order to develop the prototype by using FPGA platform. Through the procedure mentioned, the steps and stages of the process are:

### *3.1 Detection of Mails by IR Sensor*

An infrared sensor is an electronic device that emits in order to sense some aspects of the surroundings. An IR sensor will be attached at the bottom of the mailbox at the pre-cut hole. The distance of detection is adjusted to just 3cm in order to suit the application. When there is mail, despite the number, inside the mailbox, it blocks the infrared wave that emitted by the IR sensor and reflect it back to the receiver. This output a "HIGH" to the Yellow LED.

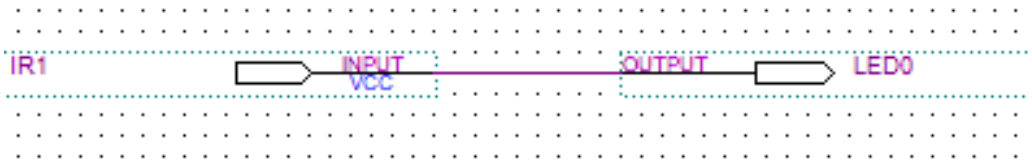


**Fig. 2.** Block Diagram of circuit involving IR Sensor

### *3.2 3-bit Up-Counter*

A 3-bit up-counter is designed using 3 JK flip-flops in order to count the number of times postman open the door of mailbox to insert the mails. This counter will count from $(000)_2$ to $(111)_2$ which is 0 until 7 in decimal. The PRESETs of all three JK flip-flops are always be inputted by a "HIGH" to disable it as it is an active low. The CLEARs are connected to the pushbutton of the mailbox's back door. Once the host open the back door to collect the mails, it will unpress the pushbutton so input a "LOW" to the active low "CLEAR" pin which turn the counter back to $(000)_2$ again.

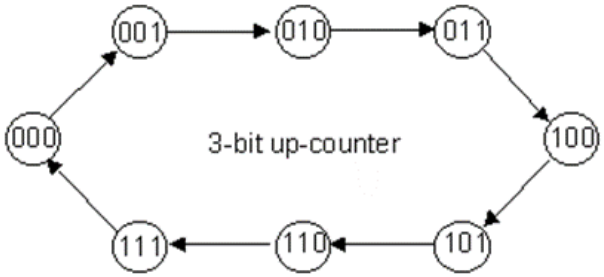


**Fig. 3.** State Diagram of 3-bit up-counter

The set of information of representation in Figure 4 can be found below,

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| J0 | = | 1 | , | K0 | = | 1 | |
| J1 | = | Q0 | , | K1 | = | Q0 | |
| J2 | = | Q0Q1 | , | K2 | = | Q0Q1 | |

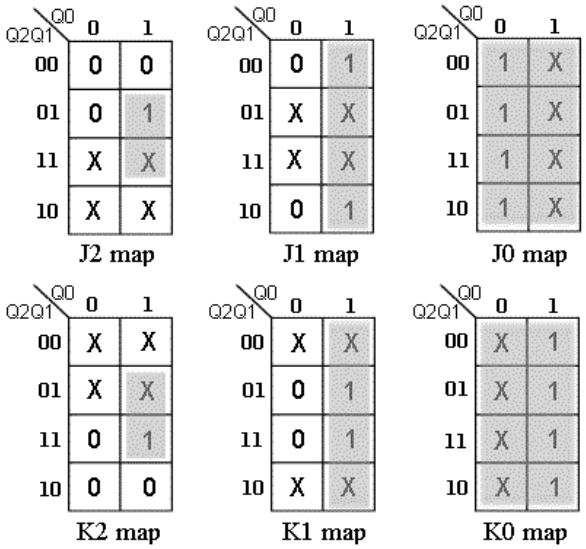


**Fig. 4.** K-maps of 3-bit Up-counter

**Table 1**
Excitation Table of 3-bit Up-counter

| Present State | | | | Next State | | | | J2 | K2 | J1 | K1 | J0 | K0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dec | Q2 | Q1 | Q0 | Dec | Q2 | Q1 | Q0 | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | X | 0 | X | 1 | X |
| 1 | 0 | 0 | 1 | 2 | 0 | 1 | 0 | 0 | X | 1 | X | X | 1 |
| 2 | 0 | 1 | 0 | 3 | 0 | 1 | 1 | 0 | X | X | 0 | 1 | X |
| 3 | 0 | 1 | 1 | 4 | 1 | 0 | 0 | 1 | X | X | 1 | X | 1 |
| 4 | 1 | 0 | 0 | 5 | 1 | 0 | 1 | X | 0 | 0 | X | 1 | X |
| 5 | 1 | 0 | 1 | 6 | 1 | 1 | 0 | X | 0 | 1 | X | X | 1 |
| 6 | 1 | 1 | 0 | 7 | 1 | 1 | 1 | X | 0 | X | 0 | 1 | X |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | X | 1 | X | 1 | X | 1 |

After K-maps done, a complete circuit diagram of 3-bits up counter is drawn as the diagram below.

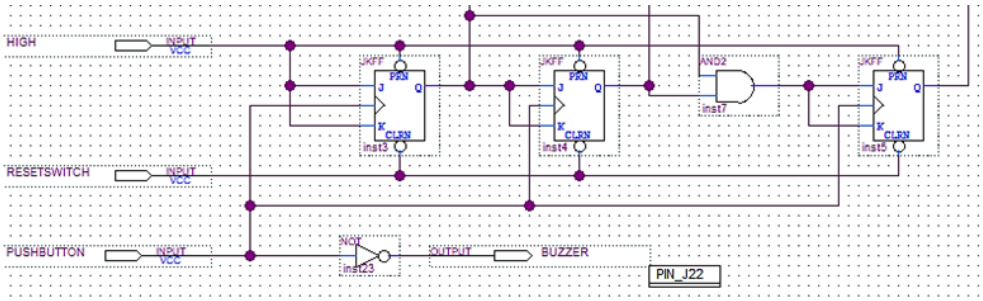


**Fig. 5.** Block Diagram of 3-bit Up-counter Circuit

There are 18 toggle switches (sliders) on the DE2 board. These switches are not debounced and are intended for use as level-sensitive data inputs to a circuit. Each switch is connected directly to a pin on the Cyclone II FPGA. When a switch is in the DOWN position (closest to the edge of the board) it provides a low logic level (0 volts) to the FPGA, and when the switch is in the UP position it provides a high logic level (3.3 volts).

Therefore, in order to provide a "HIGH" for J0 and K0, then connect an input to PIN V2 which is Toggle Switch and slide the switch to UP position all the time in order to make sure the counter function properly.

### *3.3 Stop the counter at $(111)_2$*

The Red LED lights up when the counter reaches $(111)_2$ which is 7 in decimal indicates MAXIMUM. Therefore, even if the postman continues open the mailbox and inserts the mails, the Red LED has to be lighted up until the host opens the back door to collect all the mails.

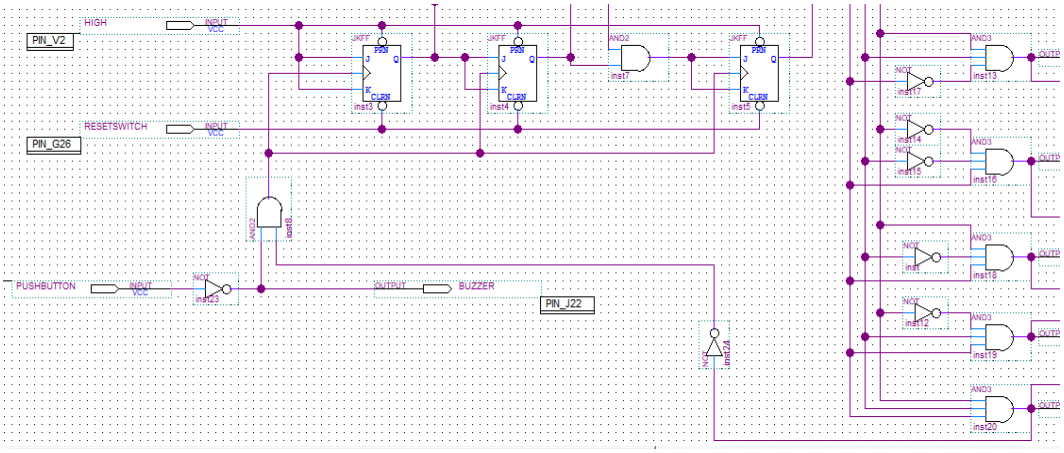


**Fig. 6**. Block Diagram showing the additional gates

In order to achieve that, the counter have to be stopped when it reached $(111)_2$. Some additional gates contribute to this application. The output $(111)_2$ is connected to a NOT gate then to a 2 inputs AND gate with another input from the front pushbutton which acts as the clock for the 3-bits up counter. Through this way, when output $(111)_2$ reached, the "HIGH" output will be transformed to "LOW" after passing through the NOT gate. Then the AND gate will not allow any signal to pass through even when the clock (front pushbutton) still activated. This condition will continue until the back pushbutton is unpressed and activate the CLEAR pin.

### *3.4 Application of Buzzer*

A 12V DC buzzer is connected to the front pushbutton and located inside the house. It acts as the output of the input signal from front pushbutton. When the front pushbutton is unpressed, which is when the postman opens the front door, it comes out with a "HIGH" output to the buzzer after passing through the NOT gate. The buzzer will stop buzzing once the postman closes up the front door. The function of the buzzer is to notify the host instantly when there is postman inserting mails into the mailbox.

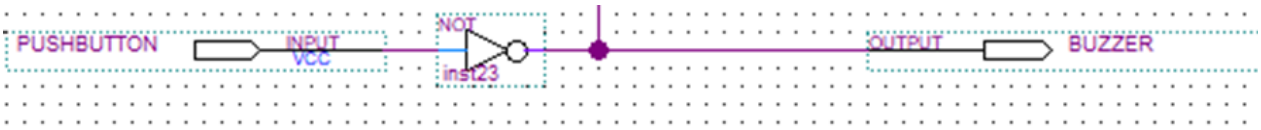


**Fig. 7.** Block Diagram showing the circuit involving buzzer application

### *3.5 7 Segment Display*

The built-in function of FPGA---7 segment display is used to display the output of 3-bits up counter. The DE2 Board has eight 7-segment displays. These displays are arranged into two pairs and a group of four, with the intent of displaying numbers of various sizes. As indicated in the schematic in figure below, the seven segments are connected to pins on the Cyclone II FPGA. Applying a low logic level to a segment causes it to light up and applying a high logic level turns it off. Each segment in a display is identified by an index from 0 to 6.

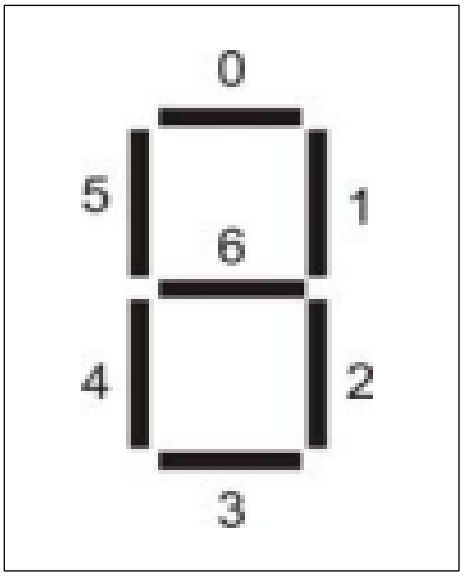


**Fig. 8.** Position and index of each segment in a 7-segment display

In this work, only 1 bit 7 segment display is used which is HEX [5]. The output of 3-bits up counter is connected to corresponding pins of 7 segment display according to the DE2 user manual. Number 1 until 7 will be displayed which is liaise to the output of 3-bits up counter $(000)_2$ to $(111)_2$. The maximum number is 7, as the counter will stop functioning when the counter reached $(111)_2$ as discussed in Part (D).

**Table 2**
Truth table for 7 segment display

| Index | | | | | | | Display |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | |

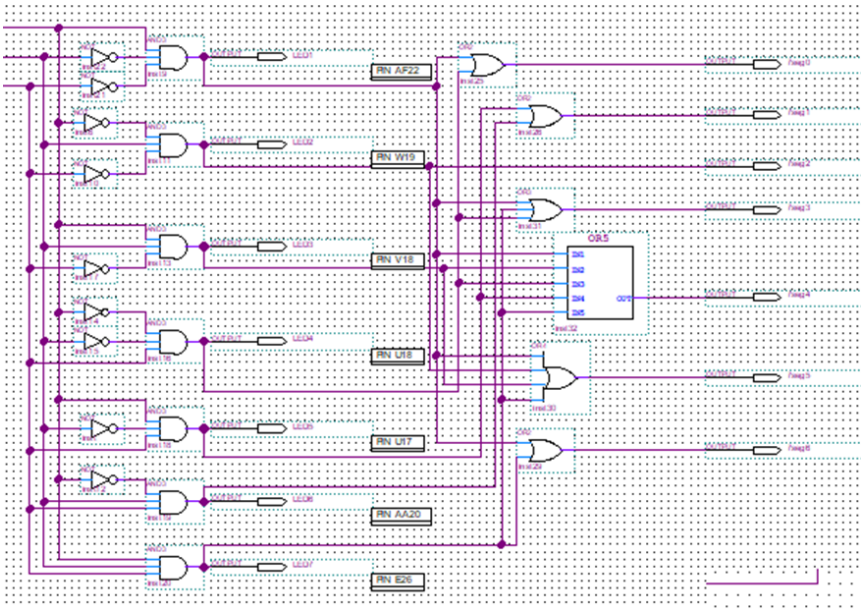

**Fig. 9**. Block Diagram for 7 segment display

### *3.6 Pushbuttons*

The DE2 board provides four pushbutton switches. Each of these switches is debounced using a Schmitt Trigger circuit. The four outputs called KEY[0], …, KEY[3] of the Schmitt Trigger device are connected directly to the Cyclone II FPGA. Each switch provides a high logic level (3.3 volts) when it is not pressed and provides a low logic level (0 volts) when depressed. Since the pushbutton switches are debounced, they are appropriate for use as clock or reset inputs in a circuit.

In this work, the use the built-in pushbuttons to represent the front and back pushbuttons. Then, the next stage is to assign KEY[2] as the front pushbutton and KEY[0] as the back pushbutton which is also the reset button.

### *3.7 Using Expansion Header*

The DE2 Board provides two 40-pin expansion headers. Each header connects directly to 36 pins on the Cyclone II FPGA, and also provides DC +5V (VCC5), DC +3.3V (VCC33), and two GND pins. Each pin on the expansion headers is connected to two diodes and a resistor that provide protection from high and low voltages. GPIO stands for General Purpose Input Output, which are connections between the FPGA and the real world.

The work uses the GPIO to connect the IR sensor, one Yellow LED, one Red LED and a buzzer. A breadboard is used for the prototype, 5V input voltage and Ground are connected to the external circuit from VCC5 and GND respectively.

## 4. Results

| Node Name | Direction | Location | I/O Bank | VREF Group | I/O Standard |
|---|---|---|---|---|---|
| 7seg0 | Output | PIN_T2 | 1 | B1_N0 | 3.3-V LV...default) |
| 7seg1 | Output | PIN_P6 | 1 | B1_N0 | 3.3-V LV...default) |
| 7seg2 | Output | PIN_P7 | 1 | B1_N0 | 3.3-V LV...default) |
| 7seg3 | Output | PIN_T9 | 1 | B1_N0 | 3.3-V LV...default) |
| 7seg4 | Output | PIN_R5 | 1 | B1_N0 | 3.3-V LV...default) |
| 7seg5 | Output | PIN_R4 | 1 | B1_N0 | 3.3-V LV...default) |
| 7seg6 | Output | PIN_R3 | 1 | B1_N0 | 3.3-V LV...default) |
| B | Output | PIN_AE12 | 8 | B8_N0 | 3.3-V LV...default) |
| BUZZER | Output | PIN_J22 | 5 | B5_N0 | 3.3-V LV...default) |
| HIGH | Input | PIN_V2 | 1 | B1_N0 | 3.3-V LV...default) |
| IR1 | Input | PIN_D25 | 5 | B5_N0 | 3.3-V LV...default) |
| LED0 | Output | PIN_F24 | 5 | B5_N0 | 3.3-V LV...default) |
| LED1 | Output | PIN_AF22 | 7 | B7_N0 | 3.3-V LV...default) |
| LED2 | Output | PIN_W19 | 7 | B7_N0 | 3.3-V LV...default) |
| LED3 | Output | PIN_V18 | 7 | B7_N0 | 3.3-V LV...default) |
| LED4 | Output | PIN_U18 | 7 | B7_N0 | 3.3-V LV...default) |
| LED5 | Output | PIN_U17 | 7 | B7_N0 | 3.3-V LV...default) |
| LED6 | Output | PIN_AA20 | 7 | B7_N0 | 3.3-V LV...default) |
| LED7 | Output | PIN_E26 | 5 | B5_N0 | 3.3-V LV...default) |
| LSB | Output | PIN_AE13 | 8 | B8_N0 | 3.3-V LV...default) |
| MSB | Output | PIN_AD12 | 8 | B8_N0 | 3.3-V LV...default) |
| PUSHBUTTON | Input | PIN_P23 | 6 | B6_N0 | 3.3-V LV...default) |
| RESETSWITCH | Input | PIN_G26 | 5 | B5_N0 | 3.3-V LV...default) |

**Fig. 10.** Pin planner

Assign all the pins that require to the inputs and outputs of the circuit using the “Pin Planner” with reference to the DE2 User Manual.

After finishing the block diagram in QUARTUS II, the circuit is compiled to check for errors. Then proceed to the uploading of programme to the FPGA board using “Programmer”. Testing of programme ran smoothly as the all the function needed performing well.

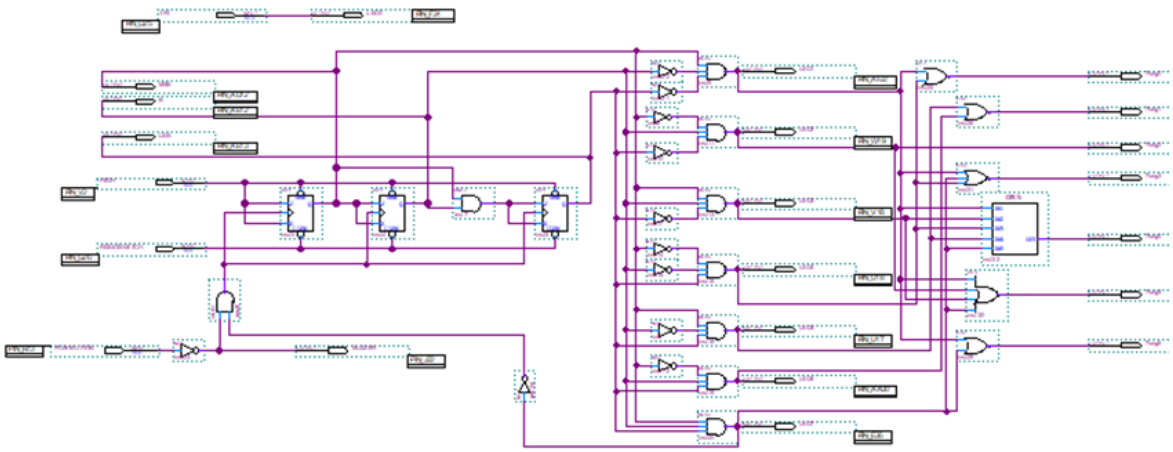

**Fig. 11.** Complete block diagram of the whole circuit

## 5. Conclusion

In conclusion, the objectives of the work are achieved. The proposed system of electronic mailbox using FPGA to detect letter has been presented. The mailbox work functionally to notify user for their new mail by buzzing the buzzer in their house, display the number mailbox opened or closed by postman and light up the LED at the mailbox. The mailbox is a user friendly, low cost and reliable. The system of the mailbox is designed using FPGA as FPGAs are reprogrammable and a concept can be verified in a hardware very fast, while in field-reconfiguration can keep up with future modifications without modifying the board layout.

However, the limitation on this system where the up- counter only counts from one until seven and stop after that. The counter won't count the number of mailboxes opened or closed by postman after the seventh times. This is because the system is designed using 3-bit up-counter that counting from one to seven. If the system is design using 4-bit or 5-bit and above, the up counter will count until fifteen, thirty-one and above respectively. As the possibility for the number of mailboxes to be opened or closed by postman in a week is low (not acceding to fifteen and above) the system is design using only 3-bits up counter and the counter will reset as the user collect their mail.

## Acknowledgement

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