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Application of Taguchi Method for Lower Subthreshold Swing in Ultrathin Pillar SOI VDG-MOSFET Device

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Abstract – *The reduction in the dimension of planar MOSFET device appears to be limited when it reaches to 22nm technology node. In this research , a new concept of MOSFET architecture named as Ultrathin Pillar Vertical Double Gate (VDG) MOSFET device was introduced and it was integrated with silicon-on-insulator (SOI) technology for better electrical performances. The virtual device fabrication and characterization were executed by using ATHENA and ATLAS modules from SILVACO Internationals. The process parameters of the device were then optimized by utilizing the Taguchi method for obtaining the lowest value of subthreshold swing (SS). The optimal result of the subthreshold swing (SS) was observed to be 58.07 mV/dec with threshold voltage (V_{TH}) of 0.408 V and a very low leakage current (I_{OFF})value of 9.374 x 10^{16} A/µm. These results are well within the predicted value of International Technology Roadmap Semiconductor (ITRS) 2013 for low power (LP) requirement in the year 2020.*

Keywords: ANOVA, SNR, subthreshold swing, Taguchi method

1.0 INTRODUCTION

Over the past decades, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has continually been scaled down in dimension. The main reason the MOSFET device has been attempted to be scaled down is to pack more and more MOSFET devices in a given chip area. The motivation of scaling down the MOSFET device is not only related to the size reduction, but also to acquire fast switching operation. It is believed that the smaller transistor possesses a better switching capability in term of its speed. An approach to reduce the size of MOSFET device will require all device dimensions, including physical gate length (Lg), effective channel length (Leff), and oxide thickness.

Producing planar MOSFET devices with very small channel length, especially for below the 22nm technology node is very challenging. The most critical electrical characteristics to be preserved are known as leakage current (I_{OFF}) and subthreshold swing (SS). An attempt of reducing the physical gate (Lg) of conventional MOSFET device has resulted in the drain region to be much closer to the source region, thereby introducing short channel effects (SCEs) which eventually lead to the increase of leakage current (I_{OFF}). A lot of researches have been done to circumvent SCEs by introducing the combination of high permittivity

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(high-k) dielectric material and metal gate. However, in this current research, traditional silicon dioxide (SiO_2) and polysilicon material are still being used by implementing Ultrathin Pillar Silicon-on-insulator (SOI) Vertical Double Gate (VDG) design concept.

The Ultrathin Pillar VDG-MOSFET device consists of a thin pillar that isolates the two gates. The purposes of double gates are to control the channel from both sides, thereby producing a better electrostatic control over the channel [1]. The vertical shape of an ultrathin silicon pillar is constructed in order to increase the drive current (I_{ON}). Since the drain region of VDG-MOSFET device is located at the top, the effective channel length (L_C) is independent with the thickness of the gate (Tg). Therefore, the SCEs will be further suppressed by ensuring the Lc is long enough to prevent the charge sharing effects between the source and the drain region. Another advantage of VDG-MOSFET device is a better integration with planar MOSFET as depicted in Figure 1 [2].

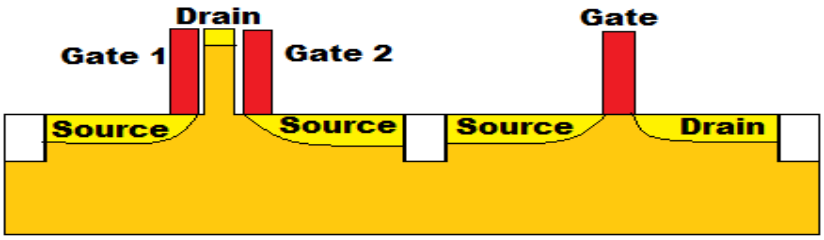

Figure 1: Integration with Planar MOSFET

In order to further suppress the SCEs, the VDG-MOSFET device is integrated with SOI technology as depicted in Figure 2. The presence of a thin silicon layer on the top of buried oxide (BOX) will create gate substrate charge coupling. The gate substrate charge coupling will contribute to higher drive current (I_{ON}), near-ideal subthreshold swing, and suppression of the floating-body effects [3]. The fast switching operation of SOI VDG-MOSFET device will be achieved due to lower subthreshold swing (SS). In order to optimize multiple process parameters in the ultrathin pillar SOI VDG-MOSFET device for obtaining the lowest subthreshold (SS) value, L_{18} orthogonal array of Taguchi method is implemented. One reported that L_{18} orthogonal array of Taguchi method has been successfully minimized the shrinkage behavior of the plastic trays [4]. Another reported that L_{18} orthogonal array of Taguchi method is capable of identifying the most significant process parameters in reducing the junction depth (Xj) and sheet resistance (Rs) in shallow PN junction formation [5]. Taguchi method is the most suitable statistical method for this design due to its ability to solve multiple process parameters optimization problems with less number of experiments [6]. Performance of Taguchi method is further enhanced by adding noise factors in order to increase the possibilities to hit a better target value.

Afifah Maheran et al. have utilized the L_9 orthogonal array of Taguchi method to optimize the process parameter variations in the 22 nm gate length MOSFET device towards the threshold voltage (V_{TH}) and leakage current (I_{OFF}) [7], [8]. Based on the results, the I_{OFF} value was able to be kept at the minimum level, thereby increased the device's speed performance [7]. The robust process recipe for the 22 nm gate length MOSFET device was succesfully predicted by the combination of signal-to-noise ratio (SNR) analysis and analysis of variance (ANOVA) [9]. The V_{TH} value after the optimization approach using Taguchi method was observed to be within the prediction range of ITRS 2011 requirements [10].

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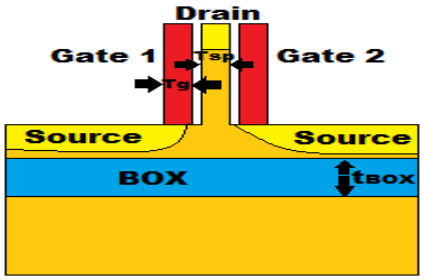

Figure 2: Ultrathin Pillar SOI VDG-MOSFET Layout

The Taguchi method relies on both signal-to-noise ratio (SNR) analysis and analysis of variance (ANOVA). The function of SNR analysis is to identify the process parameters that contain much lower noise. In fact, the level of process parameters that possesses the highest SNR will be selected as the best level as it has the strongest effect on output response. There are three types of SNR performance analysis, which are Nominal-the-best, Higher-the-better and Lower-the-better. Lower-the-better analysis type is preferred for the purpose of reducing the value of sub-threshold swing (SS). Moreover, ANOVA is executed in order to determine the percentage of factor effects towards output response. With the combination of SNR and ANOVA analysis, the best combination level of process parameters can be accurately predicted.

This paper emphasizes on utilizing L_{18} orthogonal array of Taguchi method that consists of eight process parameters which are substrate implantation dose, V_{TH} implantation dose, V_{TH} implantation energy, halo implantation energy, halo implantation tilt, source/drain (S/D) implantation dose, compensatory implantation dose and Compensation implantation energy. The gate oxide temperature and polysilicon oxidation temperature are selected as noise factors in order to get optimum results. The main objective of the current work is to minimize subthreshold swing (SS) value below 60mV/dec. Besides that, the threshold voltage (VTH) value must be within ±12.7% of low power (LP) requirement in ITRS 2013 prediction (0.447V) for the year 2020 [11].

2.0 EXPERIMENTAL

The virtual fabrication process of Ultrathin Pillar SOI VDG-MOSFET device was simulated by using ATHENA and ATLAS modules of SILVACO International. ATHENA module was used for process simulation in the device's design. Meanwhile, ATLAS module was used for device simulation and characterization.

2.1 Virtual Fabrication

The process initiated with the selection of a P-type silicon with <100> orientation as the main substrate. Next, 1 x 10^{14} atom/cm^3 of boron was implanted into the silicon substrate. Buried oxide (BOX) of 16nm (t_{BOX}) was then developed. The silicon was etched by using the retarded etching technique in order to ensure the very thin pillar with diameter of 12nm (T_{sp}) was well constructed. The ultrathin pillar was able to form a very sharp vertical channel that could tremendously increase the drive current (I_{ON}). The virtual process was followed by the gate oxidation process at temperature of 927° C. Since the device was a n-channel type, 1.81 x 10^{12} atom/cm^3 of boron was implanted into the substrate in order to form p+ region.

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After that, polysilicon material was deposited at the top of the gate oxide. Then, both polysilicon and polysilicon oxide were etched away to form a very thin gate with a diameter of 12nm (Tg). In order to optimize the performance of UTP SOI VDG-MOSFET device, indium with a dosage of 1.33 x 10^{13} atom/cm^3 was doped at an energy level of 170 Kev and tilt angle of 24^o. Halo implantation was followed by depositing sidewall spacers. Sidewall spacers were then used as a mask for source/drain implantation. An arsenic atom with concentration of 1.25 x 10^{18} atom/cm^3 was implanted in order to supply free electron to form n+ region as conductive channel.

Compensation implantation was utilized later by implanting phosphor dosage of 2.51 x 10^{12} atom/cm^3 at an energy level of 63 Kev and tilt angle of 7^o. This step is taken in order to reduce parasitic effects that could increase the leakage current (I_{OFF}). Next, silicide (CoSi) was formed at the top of the source and drain region by sputtering cobalt on a silicon surface. This transistor was then connected with aluminum metal. The aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [1], [6]. The procedure was completed after the metallization and etching were performed for the electrode formation, and the bonding pads were opened. The final Ultrathin Pillar SOI VDG-MOSFET device structure was completed by mirroring the right-hand side structure. The completed structure of the device is illustrated as in Figure 3.

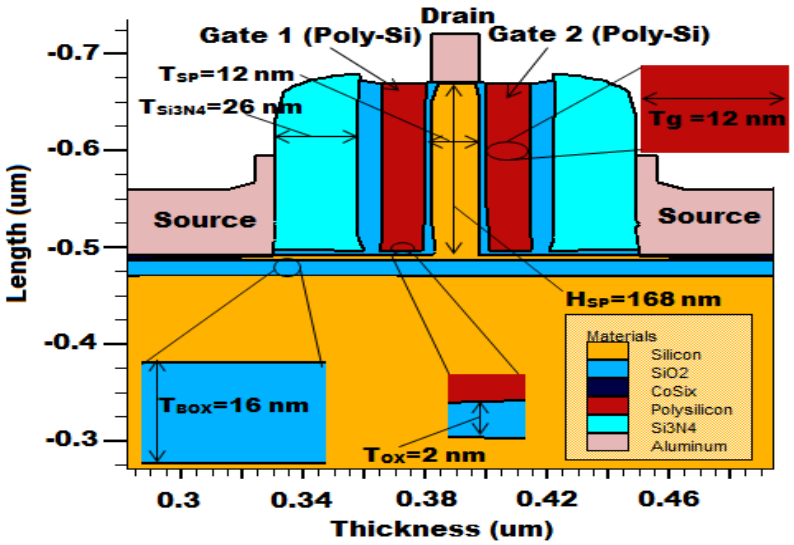

Figure 3: Structure of Ultrathin Pillar SOI VDG-MOSFET device

2.2 Taguchi L_{18} Orthogonal Array Method

The Taguchi method was utilized in order to minimize the sub-threshold swing (SS) value in Ultrathin Pillar SOI VDG-MOSFET device by attaining the best level combination of process parameters with less number of experiments. Taguchi L_{18} orthogonal array was developed in order to run 18 rows of experiment with different combination level of process parameters as enlisted in Table 1.

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Table 1: L_{18} Orthogonal Array Taguchi Method

Experiment No.	Process Parameter Level							
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**
1	1	1	1	1	1	1	1	1
2	1	1	2	2	2	2	2	2
3	1	1	3	3	3	3	3	3
4	1	2	1	1	2	2	3	3
5	1	2	2	2	3	3	1	1
6	1	2	3	3	1	1	2	2
7	1	3	1	2	1	3	2	3
8	1	3	2	3	2	1	3	1
9	1	3	3	1	3	2	1	2
10	2	1	1	3	3	2	2	1
11	2	1	2	1	1	3	3	2
12	2	1	3	2	2	1	1	3
13	2	2	1	2	3	1	3	2
14	2	2	2	3	1	2	1	3
15	2	2	3	1	2	3	2	1
16	2	3	1	3	2	3	1	2
17	2	3	2	1	3	1	2	3
18	2	3	3	2	1	2	3	1

Since the most minimum value of subthreshold swing (SS) is set as a target value, the Taguchi L_{18} (3^8) orthogonal array involving eight process parameters at three different levels with two noise factors included. Therefore, a total of 72 runs are required to optimize the process parameters in Ultrathin Pillar SOI VDG-MOSFET device. All the values of process parameters and noise factors with their corresponding levels are enlisted in Table 2 and Table 3.

Table 2: Process Parameters and Their Levels

Sym.	Process Parameter	Units	Level 1	Level 2	Level 3
A	Substrate Implant Dose	atom/cm^3	1E14	1.03E14	-
B	V_{TH} Implant Dose	atom/cm^3	1.81E12	1.84E12	1.87E12
C	V_{TH} Implant Energy	kev	20	21	22
D	Halo Implant Energy	kev	170	172	174
E	Halo Implant Tilt	degree	24	27	30
F	S/D Implant Dose	atom/cm^3	1.22E18	1.25E18	1.28E18
G	Compensation Implant Dose	atom/cm^3	2.51E12	2.54E12	2.57E12
H	Compensation Implant Energy	kev	60	62	64

Table 3: Noise Factors and Their Levels

Sym.	Noise factor	Units	Level 1	Level 2
U	Gate Oxidation Temperature	C	927	930
V	Polysilicon Oxidation Temperature	C	870	873

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3.0 RESULTS AND DISCUSSION

Based on the previous section of virtual fabrication steps, the results of the device characterization were obtained by utilizing ATLAS module. After that, Taguchi modeling was implemented in order to obtain the lowest possible value of subthreshold swing (SS). Figure 4 depicts the contour mode of Ultrathin Pillar SOI VDG-MOSFET device which indicating the device's doping profile.

3.1 Characterization of SOI VDG-MOSFET device

Figure 5 shows the graph of subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05V and V_D = 1.0V for SOI vertical DG-MOSFET device. The value of off-leakage current (I_{OFF}), drive current (I_{ON}) and subthreshold swing (SS) can be extracted from the graph.

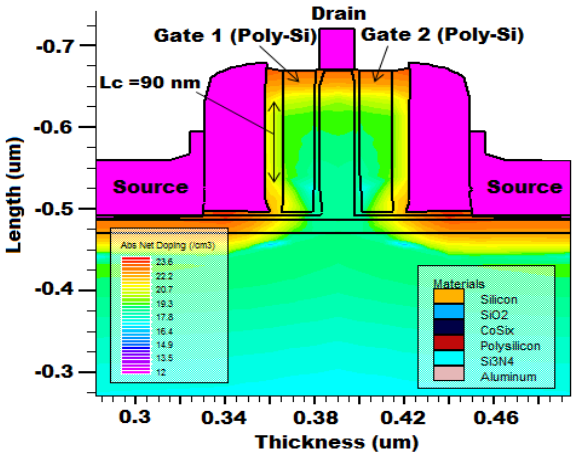

Figure 4: Contour Mode of SOI VDG-MOSFET device

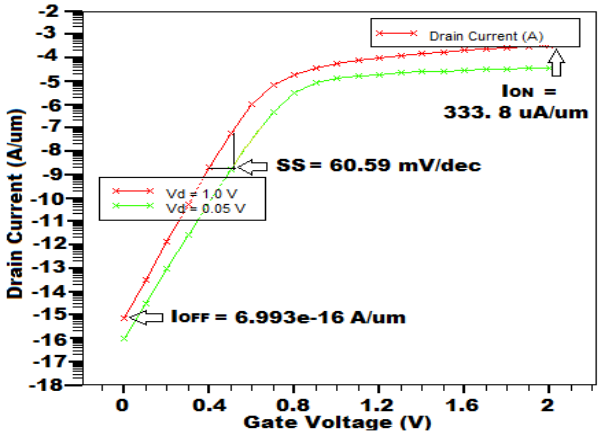

Figure 5: Graph of subthreshold drain current (I_D) versus gate voltage (V_G)

From the graph, it was observed that the value of drive current (I_{ON}) was at 333.8 µA/µm. The high drive current (I_{ON}) is needed for high speed switching operation. Meanwhile, the off-leakage current (I_{OFF}) was observed to be at 6.993 x 10^{-16} A/ µm. Finally, the initial value of subthreshold swing (SS) was extracted by using (1) [12]:

$$SS = \left[\frac{dV_{GS}}{d(\log_{10} I_{DS})} \right] \quad (1)$$

The value of subthreshold swing (SS) was observed to be 60.59 mV/dec. The subthreshold swing (SS) was the electrical response that had been selected to be optimized by using Taguchi method.

3.2 Signal-to-noise Ratio (SNR) Analysis

The L_{18} orthogonal array analysis of output response, subthreshold swing (SS) was simulated and recorded in Table 4. After obtaining all the results, process parameters of Ultrathin Pillar SOI VDG-MOSFET device were statistically modelled by using Taguchi method. Taguchi method was assigned to analyze the subthreshold swing (SS) values using SNR analysis of Lower-the-better. The SNR (Lower-the-better), η_{LTB} can be expressed as [13]:

$$\eta_{LTB} = -10Log_{10}\left[\frac{1}{n} \sum_{i=1}^{n} y_i^2 \right] \quad (2)$$

where n is the number of tests and yi is the experimental values of subthreshold swing (SS). By utilizing formula given in (2), the SNR for each row of experiments were computed and recorded in Table 5.

Table 4: Subthreshold Swing Value for Ultrathin Pillar SOI VDG-MOSFET Device

Experiment no.	Subthreshold Swing , SS (mV/dec)			
	SS1 (U1V1)	SS2 (U1V2)	SS3 (U2V1)	SS4 (U2V2)
1	60.59	59.91	60.57	59.97
2	61.71	60.12	60.19	60.23
3	61.36	59.65	60.64	60.2
4	60.61	60.43	60.79	59.75
5	61.27	60.03	59.82	61.36
6	61.62	60.5	60.82	60.84
7	60.94	60.66	59.73	62.09
8	61.09	59.56	61.03	60.13
9	60.76	60.47	59.48	61.56
10	60.26	60.45	59.75	61.72
11	60.98	60.42	59.29	60.64
12	60.32	60.41	59.69	59.3
13	59.99	60.39	60.33	61.5
14	61.74	61.8	60.43	62.22
15	61.26	60.66	60.63	60.36
16	59.34	59.2	59.39	61.91
17	60.1	61.42	60.58	59.1
18	61.7	60.53	61.03	61.65

Table 5: SNR of Subthreshold Swing for Each Experiment Rows

Exp no.	Process Parameter Level								SNR , ηLTB (dB)
	A	B	C	D	E	F	G	H	
1	1	1	1	1	1	1	1	1	-35.60
2	1	1	2	2	2	2	2	2	-35.64
3	1	1	3	3	3	3	3	3	-35.63
4	1	2	1	1	2	2	3	3	-35.62
5	1	2	2	2	3	3	1	1	-35.65
6	1	2	3	3	1	1	2	2	-35.70
7	1	3	1	2	1	3	2	3	-35.69
8	1	3	2	3	2	1	3	1	-35.63
9	1	3	3	1	3	2	1	2	-35.65
10	2	1	1	3	3	2	2	1	-35.64
11	2	1	2	1	1	3	3	2	-35.61
12	2	1	3	2	2	1	1	3	-35.55
13	2	2	1	2	3	1	3	2	-35.64
14	2	2	2	3	1	2	1	3	-35.78
15	2	2	3	1	2	3	2	1	-35.67
16	2	3	1	3	2	3	1	2	-35.56
17	2	3	2	1	3	1	2	3	-35.61
18	2	3	3	2	1	2	3	1	-35.74

Based on SNR analysis, the performance of device characteristics can be precisely evaluated. In general, the experiment row, which has the highest SNR will be regarded as the best combinational level of process parameters. From Table 5, it can be observed that row 12 has the highest SNR value which is -35.55 dB. This indicates that the experiment of row 12 possesses the best insensitivity for the subthreshold swing (SS) value. Since the design of experiment (DoE) is orthogonal, the SNR of each process parameters can be separated out.

Based on column A, B, C, D, E, F, G and H in Table V, it is observed that all three levels of every process parameters are equally represented in 18 experiments. Thus, the average of all *ni* values can be computed and expressed by [13]:

$$m = \frac{1}{n}\sum_{i=1}^{n} n_i \tag{3}$$

where *ni* is the mean SNR for *ith* experiment. In other words, m is a balanced overall mean over the entire experiment region. Besides that, the SNR of each process parameters for certain level can be separated out by [13]:

$$m_{Xj} = \frac{1}{n_j}\sum_{i=1}^{n_j} n_{ji} \tag{4}$$

where X is the symbol of process parameters and j is the level of factor. For instance, level 1 of factor A is selected to be analyzed in term of average SNR. From Table V, it can be observed that factor A was at level 1 for row 1 to row 9. The average SNR for level 1 of factor A is denoted by mA1 and expressed by:

$$m_{A1} = \frac{1}{9}\left[\eta_{LTB1} + \eta_{LTB2} + \eta_{LTB3} + \ldots\ldots + \eta_{LTB9}\right] \tag{5}$$

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The same procedure was applied to all levels and process parameters. The SNR (Lower-the-better) for each level of process parameters with a total mean of SNR is summarized in Table 6.

Table 6: SNR of Process Parameters in Ultrathin Pillar SOI VDG-MOSFET Device

Process Parameters	SNR (Lower-the-better), mXj			Overall Mean SNR, m
	Level 1	Level 2	Level 3	
A	-35.65	-35.65	-	
B	-35.61	-35.68	-35.64	
C	-35.63	-35.65	-35.66	
D	-35.63	-35.65	-35.66	-35.65
E	-35.69	-35.61	35.64	
F	-35.62	-35.68	-35.63	
G	-35.63	-35.66	-35.65	
H	-35.66	-35.63	-35.65	

Based on the data in Table 6, the factor effects graph for SNR (Lower-the-better) is plotted as illustrated in Figure 6. The dashed horizontal lines in the graph represent the overall mean of SNR (Lower-the-better) which is -35.65 dB. From the graph, it can be observed that factor A2, B1, C1, D1, E2, F1, G1 and H2 have been selected as the optimum value due to their higher SNR. Factor A, B, C, D, E, F, G and H represent Substrate Implantation Dose, V_{TH} Implantation Dose, V_{TH} Implantation Energy, Halo Implantation Energy, Halo Implantation Tilt, S/D Implantation Dose, and Compensation Implantation Dose and Compensation Implantation Energy respectively.

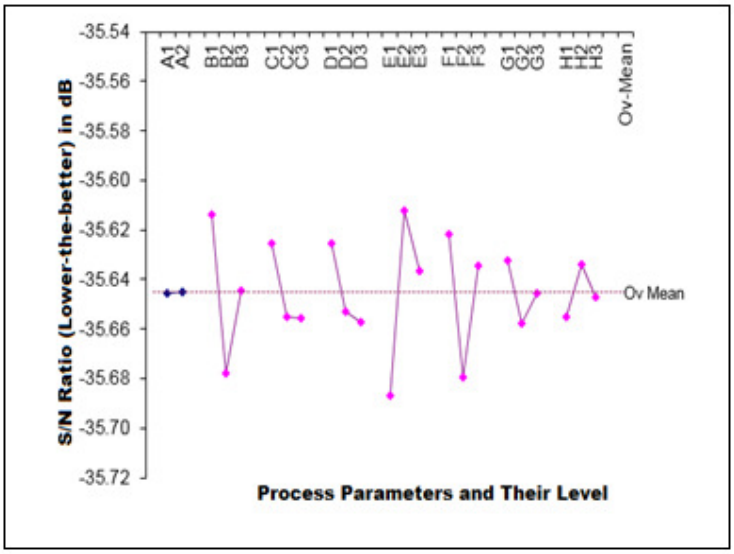

Figure 6: Factor effect plot for SNR (Lower-the-better)

3.3 Analysis of Variance (ANOVA)

The Taguchi method involves an analysis that is capable of revealing which factors are the most effective in reaching the target value and the directions in which factors should be

adjusted to improve the results. The analysis of variance (ANOVA) is a common statistical technique to determine the percent contribution of each factor that could significantly affect the sub-threshold value swing (SS) in Ultrathin Pillar SOI VDG-MOSFET device.

ANOVA consist of parameters such as degree of freedom (DF), sum of square (SSQ), mean square (MS) and percentage of factor effects on SNR. The degree of freedom (DF) of tested process parameters is computed by [14]:

$$DF = t - 1 \tag{6}$$

where t is the repetition of each level of the process parameters, p. DF represents the number of observations used in the variance (mean square) calculation. The sum of square (SSQ) is a measure of deviation of the experimental data from the mean value of the data. The total sum of squares can be calculated as [13]:

$$SSQ_T = \sum_{i}^{n} (n_i - m)^2 \tag{7}$$

Sum of square for each process parameter (SSQρ) is defined as the sum of square of average performance of a process parameter at each level, expressed by:

$$SSQ_{p(X)} = k\left[\sum_{j=1}^{k} (m_{Xj} - m)^2\right] \tag{8}$$

where X is the symbol of the process parameter (factor), k is the number of factors, j is the level of process parameter and mXj is the effect of a factor level. The variance (mean square) of process parameter tested is computed by [13]:

$$V_p(MS) = \frac{SSQ_P}{DF} \tag{9}$$

F-value for each process parameter is the ratio of variance due to the effect of a process parameter and variance due to error term, expressed by:

$$F_p = \frac{V_P}{V_e} \tag{10}$$

F-value is utilized to measure the significance of the process parameter with respect to the variance of error, Ve of all process parameters. Normally, the large F-value will greatly affect the device characteristics due to the variability of process parameters [10].

The percent contribution of each process parameter is the ratio of the process parameters sum of square (SSQ_P) to the total sum of square (SSQ_T). For instance, the percentage contribution (ρ) due to factor A can be measured as [13]:

$$\rho_A = \frac{SSQ_{P(A)}}{SSQ_T} \times 100 \tag{11}$$

The process of ignoring an individual process parameter and then subsequently adjusting the contribution of the other process parameters is known as pooling. The results of ANOVA for Ultrathin Pillar SOI VDG-MOSFET device is presented in Table 7.

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Table 7: Results of ANOVA

Process Parameters	DF	SS	MS	F-value	Factor effect on SNR (%)
A	1	0	0	-	0
B	2	0	0	9	22
C	2	0	0	3	7
D	2	0	0	3	7
E	2	0	0	13	32
F	2	0	0	8	20
G	2	0	0	-	3
H	2	0	0	-	3

The factor effect percentage in Table 7 shows the significance of a process parameter in reducing variation in Ultrathin Pillar SOI VDG-MOSFET device. A process parameter that contributes the highest percentage of factor effect on SNR will be recognized as the most influential process parameter towards subthreshold swing (SS). The percentages of factor effect on SNR of all process parameters are visualized as in the Pareto chart in Figure 7.

Based on Figure 7 , halo implantation tilt angle is observed to be the most significant process parameter in reducing subthreshold swing (SS) value with percentage of 32%. Other significant process parameters are V_{TH} implantation dose (22%), S/D implantation dose (20%), V_{TH} implantation energy (7%) and halo implantation energy (7%). The remaining process parameters are recognized as neutral as they do not have much effect on subthreshold swing (SS) value.

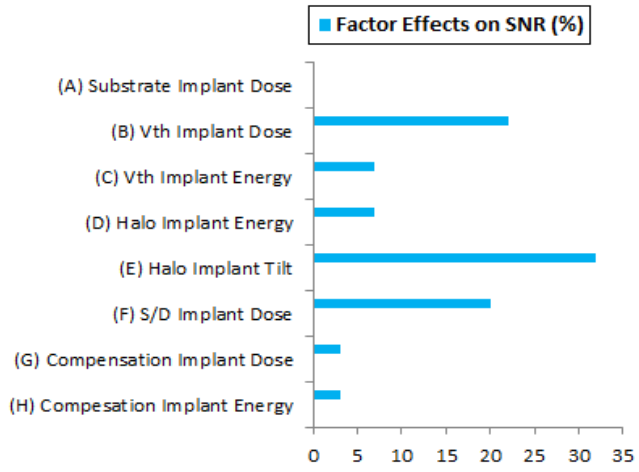

Figure 7: Pareto Chart of Factor Effects on SNR

4.0 VERIFICATION TEST

Verification test is implemented in order to justify the results retrieved by using Taguchi method analysis. Based on the results in Table 6 and Figure 6, the highest SNR value for each process parameter level to obtain the minimum value of subthreshold swing (SS) can be discovered. Before the optimization approach, the best combination level of process parameters was observed to be factor A2, B2, C3, D2, E2, F1, G1 and H3 with SNR of -35.55 dB as listed in experiment row 12 in Table 5. After the optimization approach, the best

combination level of process parameters was observed to be factor, A2, B1, C1, D1, E2, F1, G1 and H2 as listed in Table 8.

Table 8: Best Combination Level of Process Parameters

Sym.	Process Parameter	Units	Best Value
A	Substrate Implant Dose	atom/cm^3	1.03x10^{14}
B	V_{TH} Implant Dose	atom/cm^3	1.81x10^{12}
C	V_{TH} Implant Energy	kev	21
D	Halo Implant Energy	kev	1.70x10^{13}
E	Halo Implant Tilt	degree	27
F	S/D Implant Dose	atom/cm^3	1.22x10^{18}
G	Compensation Implant Dose	atom/cm^3	2.51x10^{12}
H	Compensation Implant Energy	kev	62

The value of SNR (Lower-the-better) of subthreshold swing (SS) for Ultrathin Pillar SOI VDG-MOSFET device was observed to be in the range of the predicted SNR where the range is between -35.46 dB and -35.58 dB. Besides that, the value of SNR (-35.52 dB) after an optimization approach was higher than any experiment row in Table V. The verification test was then run by utilizing ATHENA and ATLAS module. The lowest subthreshold swing (SS) value obtained was 58.07 mV/dec where the optimum noise factor was identified as 927^o for gate oxidation temperature and 870^o for polysilicon oxidation temperature as shown in Table 9.

Table 9: Optimum Results of Subthreshold Swing Value

Subthreshold Swing, SS (mV/dec)				SNR (Lower-the-better) in dB
SS1 (U1V1)	SS2 (U1V2)	SS3 (U2V1)	SS4 (U2V2)	
58.07	58.59	60.6	61.37	-35.52

The minimum value of subthreshold swing (SS) was successfully achieved by using Taguchi method along with nominal threshold voltage (V_{TH}) of 0.408 V (±12.7% of ITRS 2013 prediction), very low leakage current (I_{OFF}) of 9.374 x 10^{16} A/µm, and high I_{ON}/I_{OFF} ratio of 3.53E11. Table-10 shows the comparison of the optimal SS value after the optimization approach with the SS value before the optimization approach and the SS value from previous researches. It can be observed that there was a slight improvement of 4.16% in the SS value when the Taguchi method was utilized for optimization purpose.

Table 10: Comparison of the Optimal SS Value with the Previous Researches

Subthreshold Swing (mV/dec)			
Results from this work (Before optimization)	Results from this work (After optimization)	Results from Saad et al. (2011) [15]	Results from Rahul et al. (2014) [16]
60.59	58.07	83	63.74

5.0 CONCLUSION

In conclusion, the lowest possible value of subthreshold sing (SS) of Ultrathin Pillar SOI VDG-MOSFET device was successfully predicted and modelled by using SILVACO International simulation software and Taguchi method. The device was virtually designed by utilizing ATHENA module in SILVACO TCAD. The electrical characteristics of the device were then extracted by using ATLAS MODULE. After discovering the ideal recipe for the device, Taguchi method was implemented in order to optimize the level of input process parameters towards the subthreshold swing (SS) value with less number of experiments. The level of significance of each input process parameter on the subthreshold swing (SS) was determined by using ANOVA. Based on the ANOVA method, V_{TH} implantation dose (22%), S/D implantation dose (20%), V_{TH} implantation energy (7%) and halo implantation energy (7%) have been recognized as the most significant factors. The minimum value of subthreshold swing (SS) was observed to be 58.07 mV/dec with nominal threshold voltage (V_{TH}) of 0.408 V (±12.7% of ITRS 2013 prediction), very low leakage current (I_{OFF}) of 9.374 x 10^{16} A/µm, and SNR of -35.52dB. A very high I_{ON}/I_{OFF} ratio (3.53E11) indicates the low power consumption of the device. Therefore, the L_{18} Taguchi method was proven to be an effective method to reduce subthreshold swing (SS) value in SOI VDG-MOSFET device.

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