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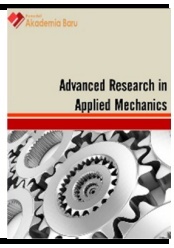

Low Power 7 nm FinFET based 6T-SRAM Design

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ABSTRACT

FinFET based SRAM design makes the SRAM more appealing in the low power applications. This paper presents a 7 nm FinFET device characterization utilizing the compact model BSIM-CMG. In addition, the paper provides simulations for different stability parameters, access time, and standby power of two 6T-SRAM cells designs consisting of different fin count. The standby power for both cells are 149 and 198 pW/µm with better read stability for the later design while the access time is constant for both cells (30 ps). The read/write operation of the two SRAM cells is stable with reducing the power supply to 0.5 V.

1. Introduction

The driving force of electronics industry is reaching better performance with very high level of integration keeping up with Moore's law [1]. By scaling down the planner MOSFET the static leakage power is more significant. Moreover, the Short Channel Effects (SCEs) and power consumption for 20 nm devices attract the designers to other technologies such as FinFET technology [2]. Nowadays FinFET based SRAM is one of the attractive research area due to the high demanding for high memory capacity.

FinFET based SRAM allows for considerable area and power reduction. Though, the cell stability should be carefully considered. The cell stability during read and write are very important design parameters that must be considered to meet the read/write requirement and to minimize the percentage of operations failure. Read/ write stability is highly affected by FinFET process variation which has a great impact on the device parameters such as drive current (I_{on}), the off-state current (I_{off}), and the threshold voltage (V_{th}). Accordingly, to increase the read/write stability there are many techniques were proposed [3,4].

This paper presents a 7 nm bulk FinFET characterization using Cadence tools. The effect of varying gate Work Function (WF) on V_{th} is studied as it is directly affect the 6T-SRAM cell stability and power consumption. The simulation setup and device electrostatic characterization are

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introduced in section 2. In Section 3, the 6T-SRAM performance, standby power and stability parameters for Read and Write operations are simulated. Section 4 shows the summary and conclusion of the work.

2. 6T Finfet SRAM and Simulation Setup

2.1 7 nm Bulk FinFET Characterization

This work proposes a 6T-SRAM based on 7 nm bulk tri-gate FinFET. Fig. 1 shows the tri-gate FinFET in 3D view. The circuit is constructed using ASAP 7 nm process design kit (PDK) by Arizona State University in collaboration with ARM Research [5]. The PDK provides four types for each NMOS and PMOS transistors with different driving capability. These devices are "SLVT", "LVT", "RVT", and "SRAM", where SLVT is the highest driving capability and "SRAM" is the lowest. To meet the new designs standby and performance requirements all these devices are supporting different values of V_{th} [5]. The SRAM device is selected from the PDK due to its low leakage current which is controlled by the (WF) [5]. In addition, the device static behavior (I-V characteristics) is simulated using compact model BSIM-CMG as an industry standard simulation model [6].

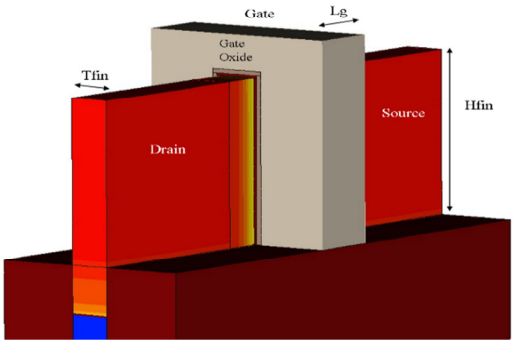

Fig. 1. 3D view of Tri-Gate FinFET

Table 1 summarizes the n-FinFET and p-FinFET nominal design parameters from the PDK model card. Fig. 2 shows the I_d-V_{gs} curve for both devices at different V_{ds} to examine their static behavior in both linear and saturation regimes. Table 2 summarizes the n-FinFET and p-FinFET DC performance at their nominal design values.

Table 1
Bulk Si FinFET nominal design parameter

	n-FinFET	**p-FinFET**
L_{gate}	20 nm	20 nm
EOT	1 nm	1 nm
H_{fin}	32 nm	32 nm
T_{fin}	6.5 nm	6.5 nm
Fin $_{doping}$	$2x10^{15}$ cm^{-3}	$2x10^{15}$ cm^{-3}
S/D $_{doping}$	$2x10^{20}$ cm^{-3}	$2x10^{20}$ cm^{-3}
S/D $_{Ext.\ doping}$	$2x10^{19}$ cm^{-3}	$2x10^{19}$ cm^{-3}
WF	4.45 eV	4.78 eV

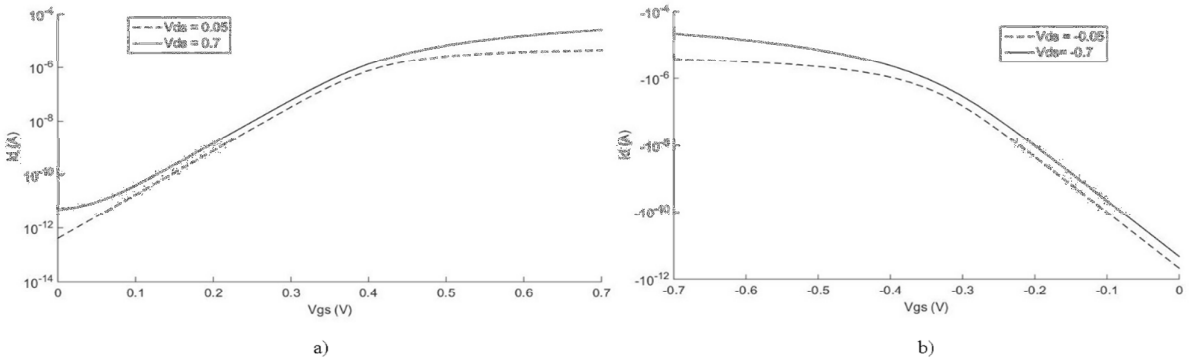

Fig. 2. I_d-V_{gs} curves for a) n-FinFET , b) p-FinFET

Table 2
7 nm FinFET I-V characteristics summary @ V_{DD}= 0.7 V

	n-FinFET	**p-FinFET**
V_{dssat}	0.7 V	-0.7 V
V_{dslin}	0.05 V	- 0.05 V
V_{th}	0.292 V	-0.266 V
I_{off}	72 pA/µm	67 pA/µm
I_{dsat}	376 µA/µm	314 µA/µm
I_{dlin}	50 µA/µm	46 µA/µm
SSwing	63 mV/dec	65 mV/dec
DIBL	25 mV/V	32 mV/V

2.2 7 nm Bulk FinFET Work Function (WF) Variation

In SRAM, the V_{th} variation is crucial due to its direct impact on the unit cell read and writes stability [7]. The most important parameters that have a major influence on V_{th} are L_g and T_{fin} [7]. The Multi-gate devices sensitivity to L_g and T_{fin} variations are captured through the BSIM-CMG model [7]. Since the Tri-gate FinFET channel is vertical, unlike the planer MOSFET, the T_{fin} variation affects the device effective width (W_{eff}) [7].

The WF is mainly adjusted to fine-tune the V_{th} value which is an effective parameter for the memory unit cell stability. Hence by increasing V_{th} the cell becomes more stable during read and write operations. Furthermore, the gate WF affects the cell access time as well [7]. As a result, design optimization must be considered to balance the cell stability and speed. The effect of WF variation on V_{th} is illustrated in Fig. 3.

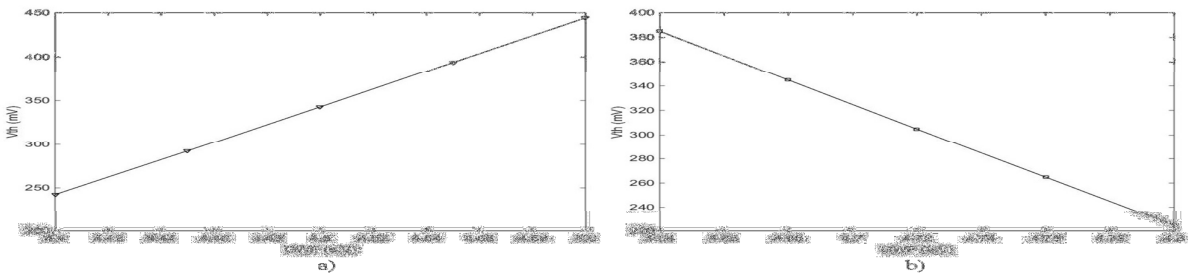

Fig. 3. Gate WF vs V_{th} for a) n-FinFET , b) p-FinFET

3. 7 nm FinFET 6T-SRAM Cell

The conventional 6T-SRAM unit cell comprises two cross-coupled inverters and two pass gate transistors (PG) as shown in Fig.4. The "SRAM" device from the ASAP PDK is utilized to construct the 6T-SRAM with the nominal design parameters in Table 1. The high V_{th} provided by the "SRAM" device is maintaining a reasonable noise margin for the read and write operations.

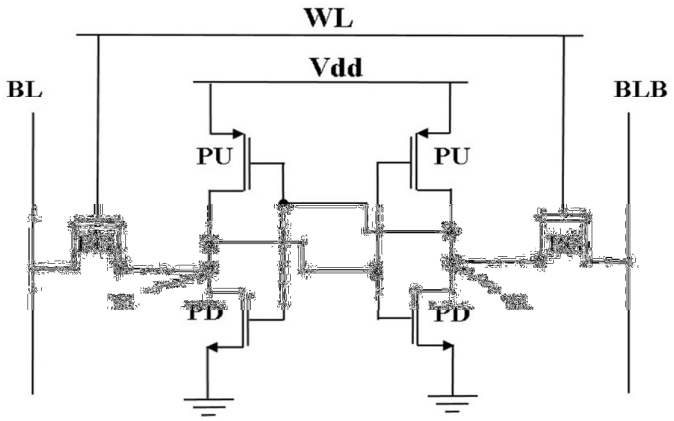

Fig. 4. 6T-SRAM circuit schematic

The constructed 6T-SRAM stability is characterized by the following key parameters

- Read stability: the SRAM stability can be measured through many static noise tests for read and write operations using the butterfly curves (BTC). It is constructed using the voltage transfer characteristic (VTC) of the cross-couple inverters. The read stability is measured by read static noise margin (RSNM). And it is evaluated from the side length of the largest square that can fit inside the BTC. If RSNM takes a negative value this means the read operation is unstable [8].
- Writing ability: for the write operation, the Bit-Line Write Margin (BLWM) is defined as the maximum bit-line voltage that can flip the cell state [9]. Moreover, the write line write margin WLWM measures the ability to lower the Word Line (WL) voltage below V_{dd} and still have successful write operation [7].

3.1 7 nm FinFET 6T-SRAM Cell Simulation Results

Two different cell configurations are constructed based on changing the number of fins per transistor for the PU, PD and PG transistors. The two configurations "111" and "121" are simulated. The first design is chosen to maintain minimum cell area, while the second for more stability [7]. The two designs are defined by the cell ratio (CR) and pull up ratio (PR). The CR is defined by the size ratio of the Pull-Drive (PD) to Pass-Gate (PG) while the PR is the size ratio of the PG transistor to the Pull-Up (PU). For cell configuration "111", the RSNM at V_{dd}.

Equals to 0.5, 0.6 and 0.7 V is shown in Fig. 5a. For the same configuration, the WLWM is shown in Fig 5b at V_{dd} = 0.7 V. Although lowering the supply voltage is an efficient technique in reducing the cell power consumption during its operation, if the unit cell is not correctly designed to handle the power supply reduction, the read or/and write operations will not function appropriately. The proper adjusting of the PR including the write assist circuits is mandatory to reduce write operation failure related to supply reduction.

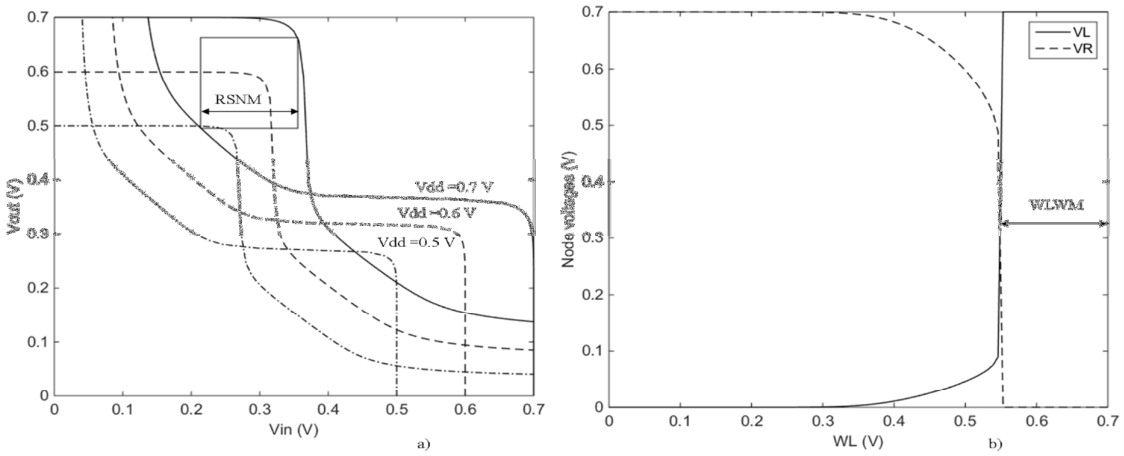

Fig. 5. 6T-SRAM a) RSNM under different supply values, b) WLWM

4. Summary and Conclusion

In this work, 6T-SRAM unit cell based on 7 nm bulk FinFET developed by Arizona State University is designed for low power applications. The read/write stability, access time and standby-power are simulated for the design. The results show that by carful adjustment of both the design parameters of the device and the unit cell aspect ratios (CR, PR) the SRAM unit cell metrics will be improved significantly. Also, the standby-power measured in hold state is lowered with supply reduction, the results are summarized in Tables 3.

Table 3
RSNM, WLWM ACCESS TIME AND STANDBY-POWER OF 6T-SRAM CELL FOR DIFFERENT CELL DESIGNS

Fin count of PU, PD&PG	**111**	**121**
L_g (nm)	20	20
RSNM (mV)	130	139
WLWM (mV)	166	164
Access time (ps)	30	30
Standby-power (pW/µm) at V_{dd} = 0.7 V	148	198
Standby-power (pW/µm) at V_{dd} = 0.6 V	127	170
Standby-power (pW/µm) at V_{dd} = 0.5 V	106	141

The results show that by increasing the fins of PD transistor the RSNM is improved. Moreover, the read/write operation is maintained stable for both cell configurations “111” and “121” even if the power supply is reduced to 0.5 V. Hence the supply voltage can be reduced by around 26% while the read/write operation stability is sustained.

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