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Fabrication and Characterization of Organic Transistors using Poly(triarylamine)-based Amorphous Semiconductor by Spin-coating Method

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Abstract – *Organic electronics is revolutionary technology aimed at unconventional electronic device on transparent substrate and will probably rely on poly(triarylamine) (PTAA) semiconductors for organic transistor fabrication. The devices described in this paper, through fabrication, measurements and extraction of transistor parameters are organic transistor having PTAA as an active semiconductor thin films by spin-coating method. The PTAA films were investigated by X-ray diffraction (XRD) to reveal the film structure orientation. The PTAA-based organic transistors exhibited a field-effect mobility (μ) of 2.68 x 10^{-2} cm^2/Vs. Tthe gate voltage operation well until -11V with the threshold voltage of 13.21V and also current on/off ratio18.23.*

Keywords: Organic field effect transistor, spin coating, Poly(triarylamine)

1.0 INTRODUCTION

In the past decade, the research for the organic field effect transistor (OFETs) has received a fast growing interest, in order to purchase their potential applications on the micro-electronics like electronic newspaper, sensor, and large area flexible display [1]. Until nowadays, a big amount of OFETs was developed and the performance can compared to the conventional transistor. However, a key problem is most of the OFETs fabricated inside the clean room or nitrogen glove box to prevent oxidise. That means that much higher cost needed in order to fabricate the OFETs.

Fabrication of the OFETs in an ambient condition was one of the solutions that can be reducing the cost. Chosen suitable organic semiconductor material is important. Poly(triarylamine) (PTAA) was the one of the well-known p type organic material [2,3]. PTAA can be dissolved in the solvent and stable to the ambient condition [3]. Furthermore, the field effect mobility of n-type organic material was lower than the p-type organic material [4]. The n-type organic material was sensitive to the atmosphere oxygen and water [4-6]

In the present study, the PTAA based OFETs with PMMA as the dielectric was fabricated. The physical characteristics such as thickness and XRD were measured. The electrical characteristics like transfer and output characteristics were measured.

2.0 DEVICE FABRICATION AND ELECTRICAL CHARACTERIZATION

OFETs with bottom gate staggered structure were fabricated on a glass substrate. The schematic cross-sectional view of the OFET is shown in Figure1. Glass substrate was soaked overnight in Decon 90 and cleaning by ultrasonic wave. An aluminum (Al) gate contact with a thickness of 300nm was deposited using DC sputtering technique. Poly(methyl methacrylate) (PMMA) was dissolved in chloroform at room temperature to form 1.0wt% solution. Then, the 380nm-thick PMMA layer was deposited by spin-coating the PMMA solution at 500rpm for 30s, followed further sintering at 4000rpm for 30s. Then, samples were annealed at 130˚C for one hour in an ambient condition. Poly(triarylamine) (PTAA) was dissolved in chloroform at room temperature to form 0.1wt% PTAA solution. Approximately 350nm-thick PTAA layer was deposited by spin coating at 500rpm for 30s, and followed further sintering at 1000rpm for 50s. Then, samples were annealed at 100˚C for 20 min in an ambient condition. Finally, Al with a thickness of 180nm as the top contact source/drain electrodes was deposited by DC sputtering technique through a shadow mask. The DC sputtering technique was carried out in Argon atmosphere of 21sccm. Figure 2 showed the image of the OFETs arrays on the glass substrate.

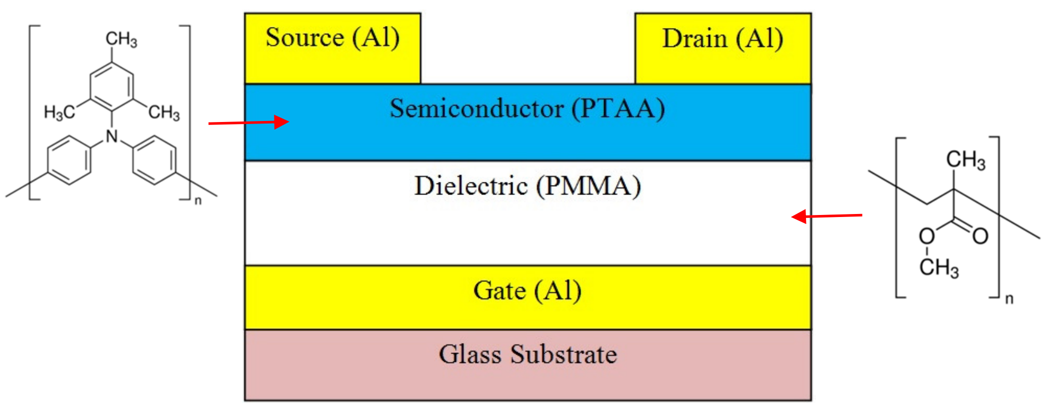

Figure 1: A schematic cross-sectional view of the OFET.

The X-ray diffraction (XRD) was carried out via X-ray diffraction instrument (X-ray Diffraction Philips Expert Pro). The thicknesses of the transistor and high resolution profiler image of PTAA were characterized via NanoMap -500LS. Meanwhile, the electrical characterization of OFETs was measured in ambient condition. Current- voltage (I-V) output characteristics of OFETs and voltage transfer characteristics were measured using a Keithley 2400 source meter unit.

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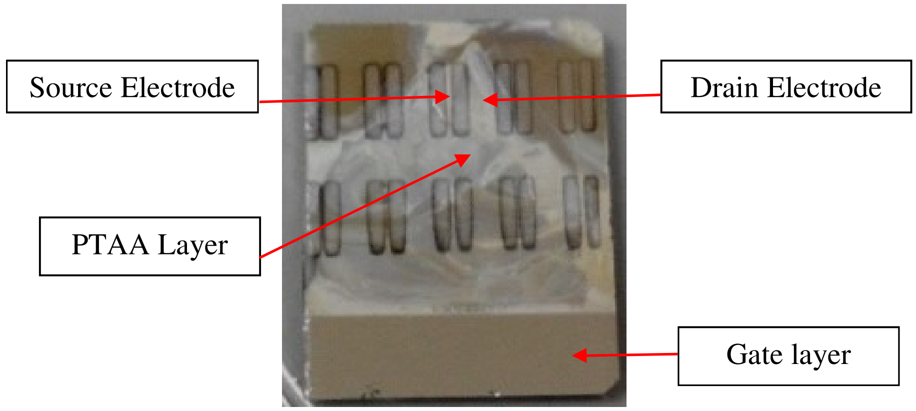

Figure 2: An image of the OFETs arrays on the glass substrate.

3.0 RESULTS AND DISCUSSION

Figure 3(a) and (b) showed the profiler image (1.5mmx1.5mm) of PTAA firm surface that on the PTAA dielectric. As shown in Figure3(a), the PTAA film showed amorphous PTAA clusters, which interference the carriers flow in the layer give rise to poor field effect mobility [7]. As shown in Figure3(b), the well-arranged PTAA polymers along semi-crystalline polymer binder line were inspected. By compared to Figure3 (a), it is clearly showed that polymers were queued and well-arranged PTAA polymers might enhance the field effect mobility of the transistors because hole of PTAA polymers easy moved. Figure 4 showed the X-ray diffraction patterns of PTAA, which partially crystalline. In Figure 4, PTAA show a peak at 23.15 ° and had satisfied interlayer stacked chain-to-chain distance. Larger interlayer distance might have lower surface resistivities [8].

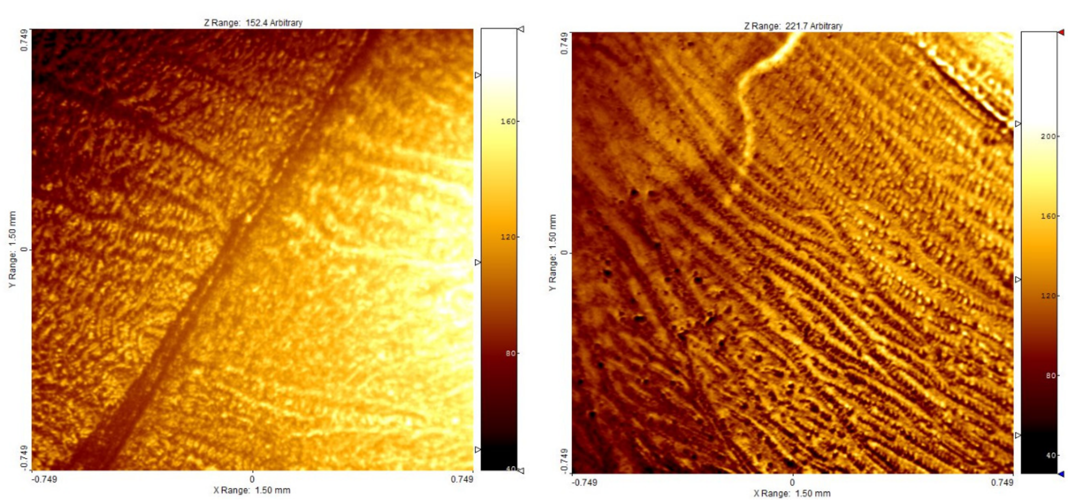

Figure 3: Profiler image of PTAA OFETs. (a) amorphous PTAA clusters. (b) well-arranged PTAA polymers.

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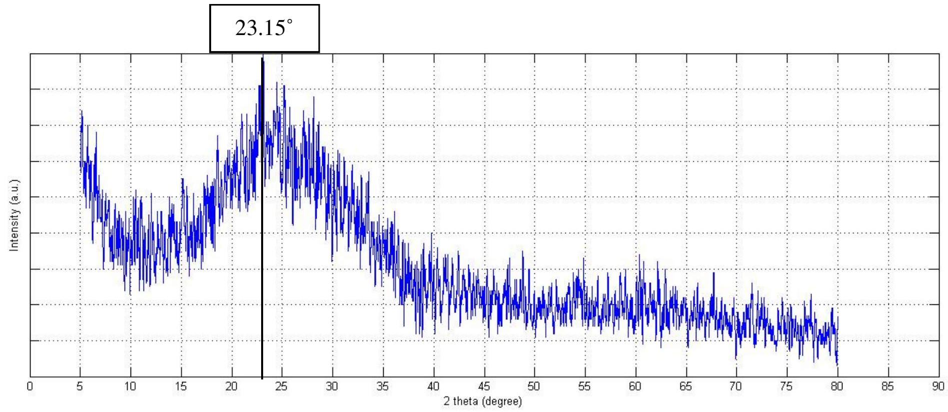

Figure 4: XRD patterns of PTAA

The capacitance per unit area (C_i) of the dielectric (PMMA) needed in order to calculate the field effect mobility (μ). C_i was calculated using the equation [1]:

$$C_i = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{1}$$

where ε_0 is absolute permittivity in free space, ε_r is the dielectric constant, d is the thickness of the PMMA. The dielectric constant of PMMA was 4.9 [9]. The capacitance per unit area (C_i) was calculated to be 11.42nF/cm^2.

The transfer characteristics of OFETs were shown at the Figure 5 and Figure 6. Due to the high internal resistivity, the drain current (I_{DS}) was low. For the whole OFETs, the gate voltage (V_{GS}) was swept from 0V to -50V, and the drain voltage (V_{DS}) was fixed at -20V. The threshold voltage of 13.21V was obtained. Field effect mobility (μ) was calculated from the slope of the |-drain current (I_{DS})|$^{1/2}$ versus Gate Voltage (V_{GS}) graph by using the equation:

$$\sqrt{I_{DS}} = \sqrt{\frac{W}{2L}\mu C_i}\,(V_{GS} - V_{th}) \tag{2}$$

where W (width) and L (length) are the semiconductor channel width and length defined by source/drain electrodes of the transistors. Ci is the capacitance per unit area of the dielectric, and Vth is the threshold voltage. The channel width and length for OFETs were 5000μm and 400μm. Field effect mobility (μ) of 2.68 x 10^{-2} cm^2/Vs was calculated from the slope of the square root of drain current versus the gate voltage (Figure 6). The subthreshold slope (SS) was calculated using the equation [1]:

$$S = \frac{\partial V_{GS}}{\partial(log I_{DS})} \tag{3}$$

The subthreshold slope (SS) and current on/off ratio were calculated approximate 57.86V/dec and 18.23. The result was decrease of two orders of magnitude of the expected result [3]. It noted that low capacitance transistor had high SS and threshold voltage, which can be attributed to the process that the charge carrier needed some electrical energy to fill trap densities before crossing the channel from source electrode to drain electrode [1].

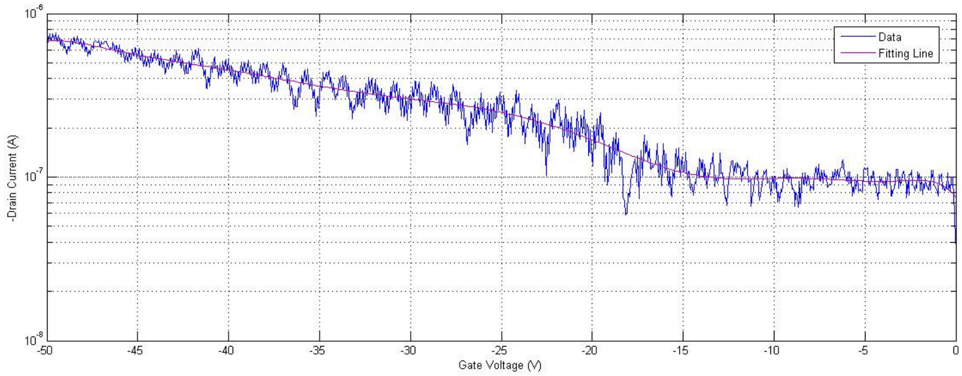

Figure 5: Log drain current (log($-I_{DS}$)) versus gate voltage (V_{GS})

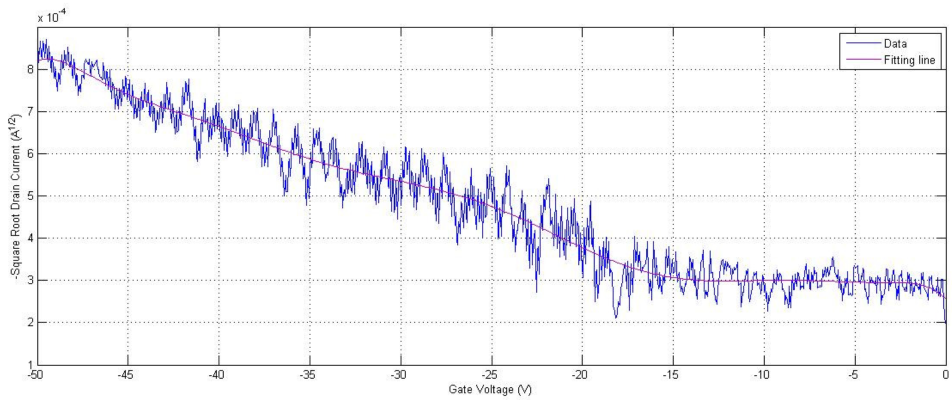

Figure 6: Square root of drain current ($\sqrt{-I_{DS}}$) versus gate voltage (V_{GS})

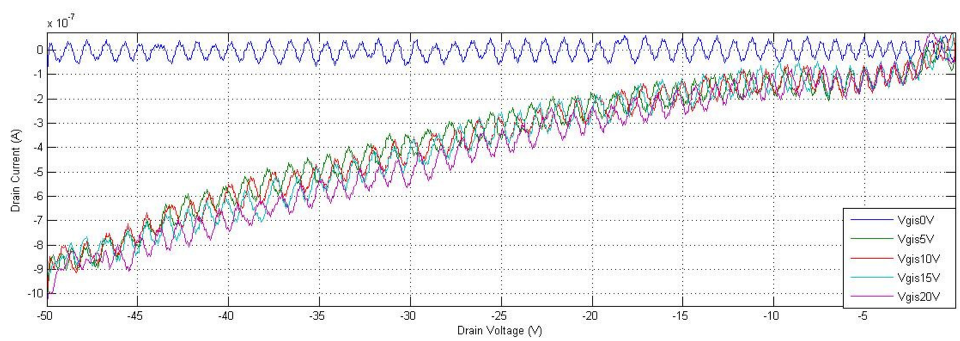

Figure 7: Output Characteristic of OFETs with Drain Voltage of 0V to -50V

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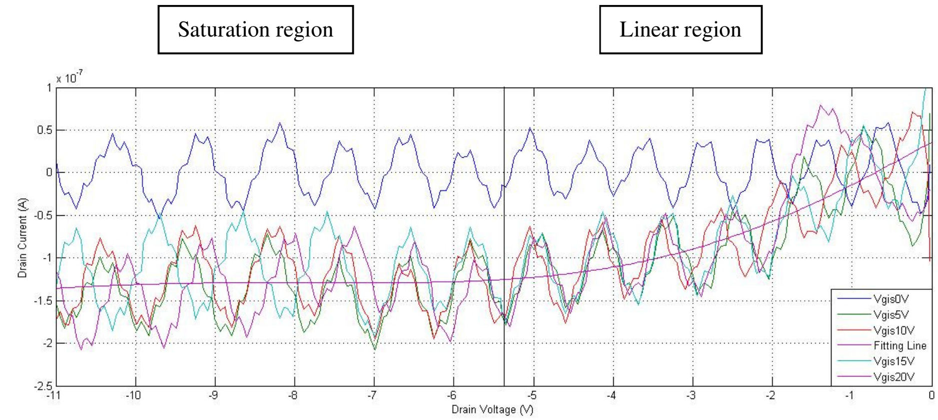

Figure 8: Output Characteristic of OFETs with Drain Voltage of 0V to -11V

Figure 7 showed the output characteristics of OFETs. For the whole OFETs, the drain voltage (V_{DS}) was swept from 0V to -50V, and the gate voltage (V_{GS}) was fixed at 0V, -5V, -10V, -15V, and -20V. It was noted there were triode mode from the 0V to-5V and saturation mode from -5V to -50V. Due to the low capacitance of PMMA, the transistors work properly at drain voltage as low as -11V (Figure 8). Form the Figure 8, the linear region was right hand side of the black straight line (-5.37V) and the saturation region was the left hand side. While drain voltage more than -11V, drain current cannot remain constant and started increase negative increment slope. It was noted that the irregular surface layer and the chemical reaction of the PTAA layer to the ambient atmosphere. By using the ohm first law, the limiting resistance was calculated approximate 16.67MΩ.

4.0 CONCLUSSION

In summary, we have successfully fabricated the PTAA-based OFETs by spin-coating method at the ambient condition. XRD pattern revealed that the semi-crystalline polymer binder line with peak at 23.15˚ which (100) diffraction axes were oriented normal to substrate plane. PTAA-based OFETs with a 11.42nF/cm^2 of capacitance per unit area exhibited threshold voltage of 13.21 V and field effect mobility (μ) of 2.68 x 10^{-2} cm^2/Vs. The OFETs function properly at -11 V of drain voltage. Further improvements in PTAA-based OFETs should be possible by decrease the thickness of dielectric layer. **REFERENCE**

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