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The Design and Characterization of Breakdown Mechanism on P+/N-Well Single Photon Avalanche Diode (SPAD)

C. W. E-Lin [*,a], *W. H. Wan Hasan*[b] *and S. Isaak*[c]

Computational and Nanotechnology Engineering Research Group (CoNE), Infocomm Research Alliance, Faculty of Electrical Engineering, Universiti Teknologi Malaysia, 81310 Johor Bahru, Malaysia

[a,*]*mroslina.kl@utm.my*, [b]*sharififoad@yahoo.com*, [c]*Davoud_sharifi@yahoo.com*, [d]*norazli.kl@utm.my*, [e]*zuritah2@live.utm.my*

Abstract – *In this paper, the breakdown voltage (VBD) and dark current (ID) of p+/n-well avalanche photodiodes operating in Geiger is reported. Simulations are performed by implemented the numerical simulations at the technological process and electrical level by using two dimensional TCAD simulations. The simulation analysis aims at relating both the VBD and ID to the relevant the device parameters, such as epitaxial layer thickness and doping concentration, in the context of device performance optimization for photon counting application. The optimized design of the Single Photon Avalanche Diode (SPAD) is included with the guard ring by the diffusion of p-wells layer to prevent the edge breakdown by limiting the high electric field at the junction periphery of the device. The result demonstrated that, the SPAD with square shape active area of 2 x 2 µm2 using low doped p-well guard ring has VBD of 27 V and IA of 0.85 pA. The simulation performances are also useful for characterization performance of silicon SPAD prior fabrication in low voltage CMOS Process.*

Keywords: Breakdown voltage, Avalanche photodiode, Geiger mode, Dark current

1.0 INTRODUCTION

In response to single photon, the suitable detectors with internal gain mechanism can significantly improve signal to noise ratio output to provide high bit rates signal processing by integrated electronic circuit. Hence that, sensors capable of detecting single photons are required for imaging system in astronomy, laser ranging, optical time-domain reflectometry (OTDR), single molecule detection, fluorescence decay, biomedical imaging and etc [1]. At present, single photon counting is available with the use optical detectors, e.g. photomultiplier tubes (PMTs), multichannel plate (MCP), charge-coupled devices (CCDs), and APDs. (PMTs) are commonly used as detectors in single photon counting of low light level signals and have been available since 1960. In PMTs, the photocathodes are available over a wide wavelength range and have high gain. PMTs usually provide good quantum efficiency in a range of 25%-30% in blue range of wavelength, especially in the visible part of the spectrum and low noise and cannot be assembled in large arrays necessary for imaging. These sensors are also very fragile and sensitive to magnetic fields that can modify the path of photoelectrons [2]. In addition, PMTs require high supply voltages in about 3 kV. In order to overcome some of these problems, micro-channel plates (MCP) were introduced. However, these devices still require large voltages and are fragile. Even though MCPs can be gated, the achievable time resolution is below that obtained with a PMT. However, due to the limitations with PMTs, MCP, and

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CCDs, avalanche photodiodes (APDs) operated above their reverse breakdown voltage in the so-called Geiger mode are used as a detector in single photon counting systems [2-5]. APDs are widely used in both industrial and research applications for the detection of low light level detection using the internal gain provided by the impact ionization process. In general, APDs have the typical advantage of combining a single photon sensitivity, low power consumption, small size, reliability, suitability to build the integrated systems and fast timing capabilities. Silicon APDs have a good feature as detectors of visible and infrared radiation (λ<1000 nm). The internal gain for APDs operating in linear mode regime is not sufficient to detect the single photon arriving, otherwise the single photon is efficiently detected by APDs operating in geiger mode, termed as single photon avalanche diodes (SPADs) [1, 4].

SPADs are able to determine photon arrival times with an accuracy of only few picoseconds and have been used as stand- alone detectors for several decades. SPADs were first successfully integrated into a modern small geometry standard CMOS processes in 2003 by using a p+-n-well SPAD junction with a p-well guard ring structure [1, 2]. However, these devices type in advanced nanoscale CMOS processes have very high doping concentrations on both sides of the active junction, which leads to high electric field. Unfortunately, this results in excessive noise due to band-to-band tunneling which generally gets worse with the increased doping concentrations required by shrinking transistor geometries [5]. Devices of this typical SPAD structure have been also reported in many generations of CMOS process [3, 4], including 90 nm with an n+-n-well structure [5].

In this paper, the design and charaterization of silicon SPAD design with p+/n-well/p-substrate junction with Silvaco TCAD simulation tool is presented. The main feature of the SPAD design is to prevent the premature breakdown at the edge of the junction, which is reversely biased at the voltage higher than its breakdown voltage. The high field multiplication region is the junction between the n-well and a thin p-epitaxial layer on a low resistivity p-substrate.

In order to bias SPAD at the voltage higher than its reverse breakdown voltage, a guard ring of p-well layer is diffused to prevent premature breakdown at the edge of the SPAD by limiting the high electric field at the junction periphery of the device. A high electrical field surrounding the junction will ensure the Geiger mode operation in the central part of the SPAD. This structure was adopted from the previous works on the SPAD design and characterization by [6, 9, 10], however the previous works used the CMOS 0.35 μm and 0.5 μm n-well process. The present study aims to enhance the electrical performance of the SiSPAD by utilizing optimal layout structure by TCAD simulations. Therefore, high breakdown voltage and minimum leakage current can be obtained with low voltage CMOS process. The simulation in defining the breakdown mechanism of the proposed SPAD structure is implemented to compare with experimental and simulation results which from the other researchers in high voltage and low voltage CMOS process.

2.0 METHODOLOGY

2.1 Operation principle of SPAD

SPAD is a reverse biased p-n junction photodiode that operate at high electric field to achieve an internal gain. In reverse biased p-n junction photodiode, valence band as depicted in Figure 1 (at point 2), an electron ionizes an atom creating another electron-hole pair, and each of newly generated electron or hole will be involved in the ionization process of further electron-hole pairs by a mechanism called avalanche multiplication. The energy required by an electron to

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ionize an atom is supplied by the kinetic energy of the electron at high electric field [1, 3, 7].

The ionization process can be characterized by a pair of ionization coefficients αp for holes and αn for electrons, respectively. Where,

αp : Number of electron-hole pairs created per hole per length travelled in the direction of the electric field.

αn : Number of electron-hole pairs created per electron per length travelled in the direction of electric field.

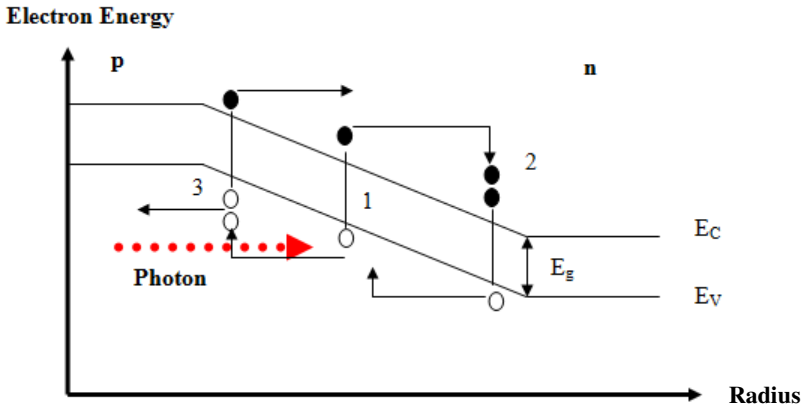

Figure 1: The multiplication process of APD [3, 10]. A black circle represents an electron; a white circle is for a hole.

The ability of an electron or a hole to trigger ionization is depends on the ionization coefficients. The ionization coefficients are strongly increase with the increasing of the electric field and decrease with temperature. The increase of the ionization coefficients by electric field is due to the acceleration of electron. It is decrease when temperature is increase due to an increasing of frequency during collision process, which decreases the probability of a carrier gaining enough energy to cause ionization. The avalanche phenomenon is quantified by two factors. The first factor is the carrier ionization rates which defined as the number of electron-hole pairs produced by a carrier per unit distance travelled. The second factor is the rate at which electrons and holes leave the high electric field region and readily collected at the electrode of the device. The ionization rates are strongly depending on the electric field. Even though the silicon electrons have higher ionization rate as compared than holes, but the average electric field about 3×10^5 Vcm^{-1} is required to create one electron-hole pair per 1 μm travelled [3, 7, 10].

To understand the linear mode operation of SPAD, a simple comparison with the geiger mode SPAD is required. The linear mode SPAD biased below the breakdown voltage. At this mode of operation, the extraction rate balances the ionization rate. Therefore, the output current and carrier concentration are increased by a gain or multiplication factor which typically between few tens and few hundreds. In linear mode SPAD, the incident light intensity is proportional to the output current. The geiger mode SPAD is biased beyond the breakdown voltage. At this regime of operation, the electric field is extremely high. Thus, the extraction rate does not balance the high ionization rate. As consequent, the output current and carrier concentration are rise swiftly to very high values, usually in the miliampere range.

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As the voltage reaches avalanche voltage, the current starts to increase due to the onset multiplication phenomenon, as illustrated in Figure 2. When the voltage exceeds the breakdown voltage, the current tends to diverge. Corresponding to the gain-voltage curve, for the case of linear mode SPAD, the gain starts being larger than 1. Meanwhile, in geiger mode SPAD, it tends to reach virtually infinite value, which practically can exceed 10^6 [7].

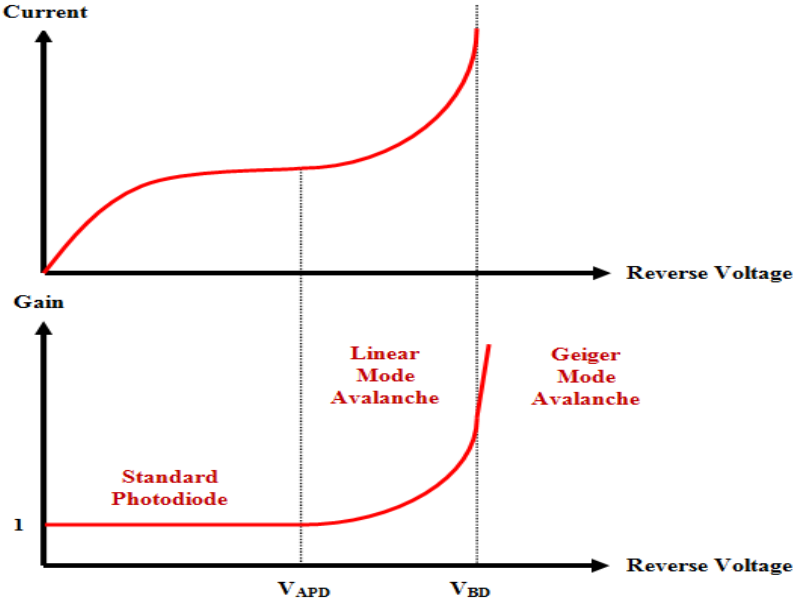

Figure 2: The characteristic of current-voltage and gain-voltage for photodiode mode, linear mode and geiger mode SPAD [7, 10].

2.2 SPAD Structure

The schematic cross section of SPAD with p+/n-well/p-substrate junction is shown in Figure 3. Various methods exist for generating SPAD and guard ring in planar processes [1-5, 8,11]. Most CMOS processes use p layer as the substrate, hence that a common SPAD uses the n+ diffusion to generate n+/p-well junction, with shallow n-well forming the guard ring. If the CMOS process has a deep n-well, the implant dopants can be reversed with the deep n-well acting as the substrate. By implementing this method, a p+ active region with p-well forms the guard ring on top of a deep n-well. A guard ring with a lower doped implant (p-well) is applied to limit the electric field at the edges of the junction and isolates the SPAD from substrate noise, since the substrate and the deep well form an additional junction that will prevent free carriers in the substrate. Thus, the premature discharge can be avoided [6, 11].

The schematic cross section of SPAD structure with the inclusion of diffused low-doped p-well as guard ring layer is illustrated in Figure 4. The active SPAD device is made inside an n-well, which acts as the cathode and the anode is formed by p+ diffusions. The p+ diffusion defines the active area where the incident light is detected. In Geiger mode, the electron-holes pairs generated due to the absorption of an incident light in the p+ diffusion area (anode) are multiplied before collected by n+ terminal (cathode) [1-4, 6-9]. It is necessary to separate the active region from surrounding area; otherwise only one large SPAD could be fabricated without electronics coupling. A guard ring structure is responsible for this separation and with no guard ring; carriers will diffuse into the active region, causing spurious avalanches where

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the edge or periphery effect can contribute to premature reverse breakdown on a reverse biased diode. A guard ring structure has been adopted to reduce the high electric field at the junction periphery of the device with a lightly doped deep p-well to avoid edge breakdown and to make a planar multiplication region. Using a deep n-well isolates the SPAD from substrate noise, since the substrate and the deep well form an additional that will prevent free carriers in the substrate [1-4, 10-13]. The diode had been design with rounded corners and is enclosed in two p-well guard rings. A p-well layer with junction depth of 1.2 µm encircling the p+ diffusion forms the guard ring on top of an n-well and was used to reduce strong electric fields.

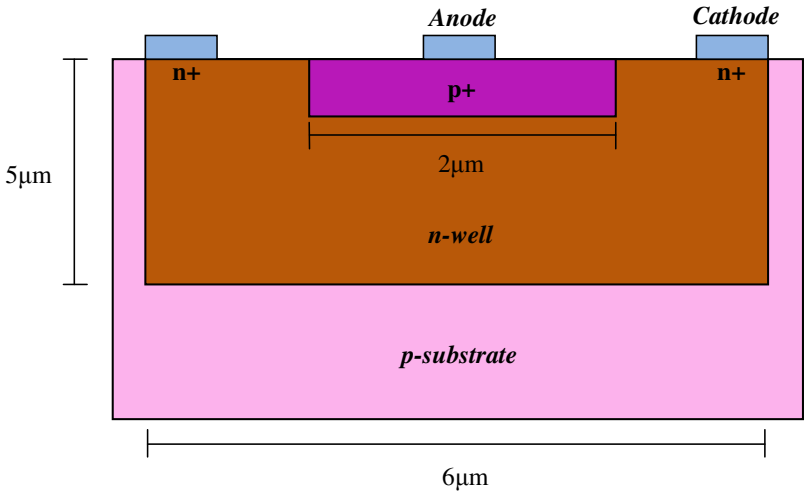

Figure 3: Schematic of cross section of SPAD without guard ring

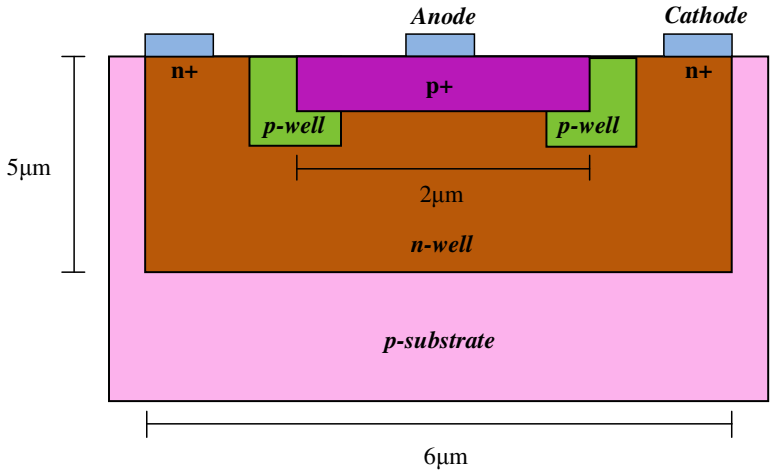

Figure 4: Schematic cross section of SPAD with a low doped p-well as guard.

3.0 RESULTS AND DISCUSSION

In an optimized SPAD, the device must exhibit two main characteristics in order to operate in Geiger mode regime. First, it must show abrupt breakdown behavior and the second is low

avalanche current. In essence, the free carriers entering the high electric field region may trigger an avalanche breakdown in Geiger mode operation. Second, the optimized structure of SPAD without guard ring is included with low doped p-well guard ring in order to prevent the premature breakdown, as well as to maximize the electric field at the center of multiplication region and to minimize the avalanche current [9, 14].

3.1 Doping Concentrations

This doping profile was simulated using Silvaco's Athena process simulator to determine the current-voltage (I-V) performance with varied process parameters. By utilizing this information, a fully optimized device can be constructed with a maximum V_{BD} and smallest I_D. Since the SPAD device has gated p-n structure, the substrate doping concentration affects the SPAD characteristics. Therefore, an optimal study on the substrate doping concentration plays an important criterion to design the SPAD device without the guard ring layer, as depicted in Figure 5, which defines the relationship between n-well doping concentration (N_d) and breakdown voltage (V_{BD}) of SPAD with arsenic doping concentrations in a range between 3 e^{14} cm^{-3} to 3 e^{16} cm^{-3}. A higher doping concentration of 3 e^{16} cm^{-3} leads to the higher V_{BD} at about 22 V. SPAD shows lower V_{BD} of 6 V and 4 V, respectively for lower doping concentration.

The effect on V_{BD} with phosphorus as n-well is depicted in the Figure 6, where for doping concentration of 3 e^{16} cm^{-3} gives V_{BD} approximately 24 V. From the observation, results show that V_{BD} is dependent upon doping concentration [10-13] with reduced doping concentrations gives V_{BD} at about 3 V and 2 V.

By using Equation (1) and Equation (2) [8-11], the result obtained from the simulation is verified. The performance based on simulations and calculations are presented as in Table 1 for arsenic and Table 2 for phosphorus.

$$E_{max} = \frac{eN_d x_n}{\varepsilon_s} \quad (1)$$

where e is a constant $=1.6\times10^{-19}$, N_d= doping concentration, x_n = depletion width, ε_s = permittivity of the material, while the depletion width is given by:

$$x_n = \left[\frac{2\varepsilon_s V_R}{eN_d}\right]^{0.5} \quad (2)$$

where V_R is the magnitude of the applied reverse bias voltage and the built in potential, V_{Bi} was neglected. If now V_R define to be breakdown voltage, V_{BD}, the maximum electric field, E_{max} will be define as a critical electric field, E_{crit}, at breakdown. Hence, the breakdown voltage, V_{BD} can be given by the Equation (3).

$$V_{br} = \frac{\varepsilon_s {E_{crit}}^2}{2eN_d} \quad (3)$$

where N_d is the semiconductor doping at low doped region of the one sided junction. Therefore, V_{BD} is actually proportional to the phosphorus concentration.

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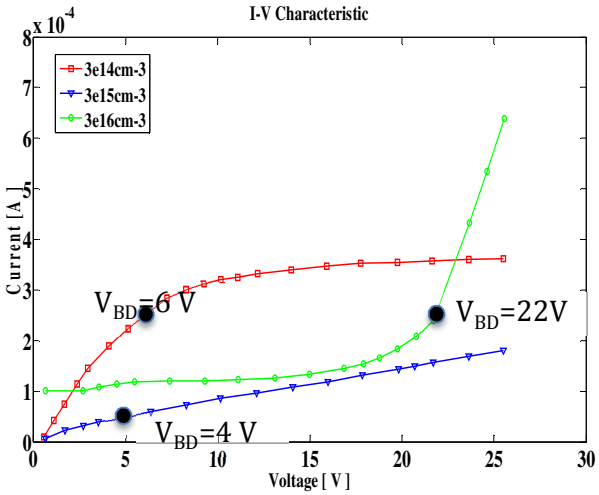

Figure 5: I-V plot of the SPAD for various arsenic doping concentration

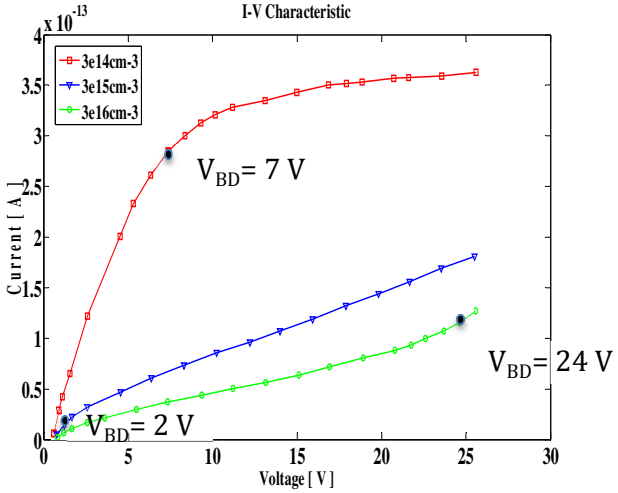

Figure 6: I-V characteristics of the APD for various phosphorous doping concentrations

The comparison data between simulated and theoretical reveals that N_d is a strong function of doping concentration. As doping concentration increase, the V_{BD} is increase, resulting a peak electric field at the depletion region of diodes. At high electric field, the individual carriers within the depletion region become the hot carriers. These hot carriers acquire adequate energy to generate electron-hole pair by colliding with lattice atoms and leads to the avalanche process. In general, for photon counting applications, SPAD must experience breakdown behavior by avalanching mechanism [12].

Therefore, the n-well doping concentration of 3.0 x 10^{16} cm^{-3} was chosen in order to have a higher V_{BD}. Low doping concentration of 3.0e^{14} cm^{-3} in both materials showed that the free carriers at the depletion region do not have enough energy to trigger an avalanche breakdown. This is due to the lower electric field at the depletion region is not sufficient to sustain impact ionization process. A higher V_{BD} for doping concentration of 3.0e^{16} cm^{-3} also proves that the

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avalanche breakdown mechanism is occurred. It should be noted that, the predominant breakdown mechanism for the SPAD is avalanche effect, where a small V_{BD} at about less or equal to 7 V, is affected by tunneling effect instead of the avalanche effect [12].

Table 1. Simulated and calculated V_{BD} with various arsenic doping concentration

Arsenic Doping Concentration (cm^{-3}), N_d	Simulated Value of Breakdown Voltage (V), V_{BD}	Calculated Value of Breakdown Voltage (V), V_{BD}
3.0×10^{14}	4 V	0.34 V
3.0×10^{15}	6 V	2.72 V
3.0×10^{16}	22 V	19.17 V

Table 2. Simulated and calculated V_{BD} with various phosphorus doping concentration

Phosphorus Doping Concentration (cm^{-3}), N_d	Simulated Value of Breakdown Voltage (V), V_{BD}	Calculated Value of Breakdown Voltage (V), V_{BD}
3.0×10^{14}	2 V	0.50 V
3.0×10^{15}	3 V	2.94 V
3.0×10^{16}	24 V	23 V

3.2 P-well implantation as guard ring layer

A major issue in SPAD design is represented by edge effects in the p-n junction, where high electric field can produce premature breakdown and therefore prevent the device to operate in Geiger mode. In order to reduce edge effects, guard rings of low-doping diffusions are employed. The purpose of the diffusion is the reduction of the electric field below the values reached in the planar multiplication region. The effect of surface fields on V_{BD} shows that the breakdown voltage can be modulated over a very wide range by the application of an external surface field and it tends to saturate at a maximum and at a minimum value as the gate voltage is varied in such a way as to deplete the lowly doped and highly doped sides of the junction, respectively. Both the high-voltage and the low-voltage saturation of V_{BD} appear to be due to the formation of field-induced junctions, which prevent further variation in the shape of the depletion region [3, 4, 8].

The electric field profile shows that a peak electric field of 500 kV/cm appears at the edge of the junction as shown in Figure 7(a). The breakdown will naturally occur at the areas with the highest electric field and may happen at the corner junction of the diode due to the high electric field strength at the edge. The optimized design of SPAD with the inclusion of diffused p-well low doped guard ring surrounds the p+ anode is able to minimize the electric field which is about 370 kV/cm at the junction curvature as shown in Figure 7 (b). By introducing the guard ring, the free carriers at the border of diode will be captured by the electric field, thus preventing the edge breakdown. The breakdown voltage is increased and the leakage current is minimized. In this design, the ion dose of p-well 10^{11} cm^{-2} is used as a guard ring. In order to implant p+

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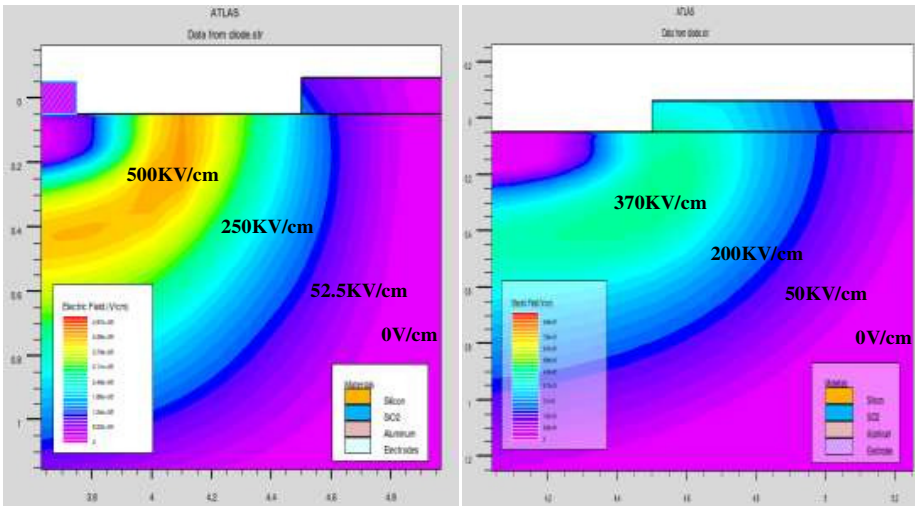
material, nitride was used as the mask to cover the place where the implant is not required. The oxide layer was deposited as the barrier between the junction and the nitride layer.



(a) **(b)**

Figure 7: TCAD simulation of electric field distribution of SPAD (a) without guard ring (b) with guard ring

Figure 8 shows the optimized schematic of SPAD, which was designed and simulated using Silvaco TCAD. The p-n junction is formed from p+ material in an n-well. However the high doping concentration of p+ and n-well use in transistor results in a thin depletion region at the junction. This effect generates large leakage current and disallowed the device to operate in Geiger mode. The thin depletion region means that carriers often cross the depletion region, an event indistinguishable from that of the arrival of a photon. This is known as dark count, as these counts are measured in the absence of photons [13]. In this design the guard ring is formed simply by the p-well has graded p-doping through it, lowering its overall doping level and therefore resulting in a good low field region, which reduces any edge-effects.

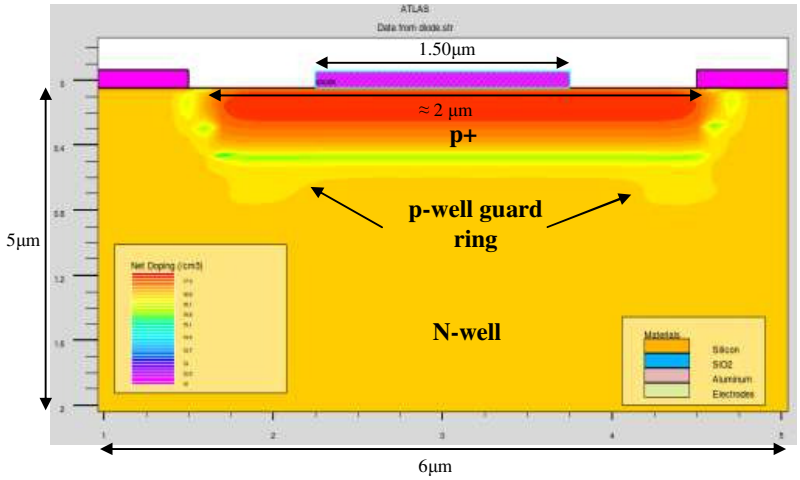


Figure 8: The schematic of proposed SPAD

The leakage current with guard ring SPAD is approximately zero until the voltage reaches the breakdown region and started to increase rapidly at 27 V, which is, assigned as V_{BD} (as depicted

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in Figure 1.9). Meanwhile, for SPAD without guard ring, the current is rise swiftly at V_{BD} of 21 V. The leakage current (I_D) for SPAD with the guard ring is about 0.85 pA at the breakdown and SPAD without guard ring contributes I_D of 0.15 mA. This finding in the same agreement with previous study on Geiger mode device [1, 6, 7, 14, 15], which is proved that a higher V_{BD} value would, minimized I_D. The I–V characteristic of SPAD without guard ring shows that V_{BD} value just below breakdown provides only a worst-case bound on SPAD dark count rate performance and limits the operation of device in linear or avalanche mode.

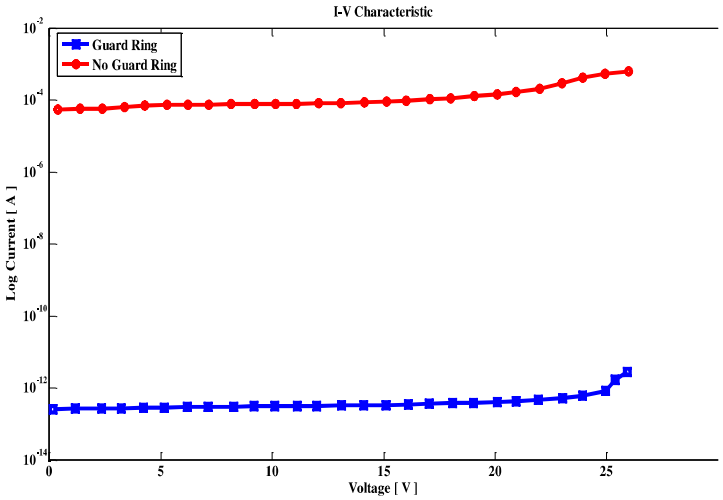

Figure 9: I-V characteristic of SPAD with and without p-well guard ring layer

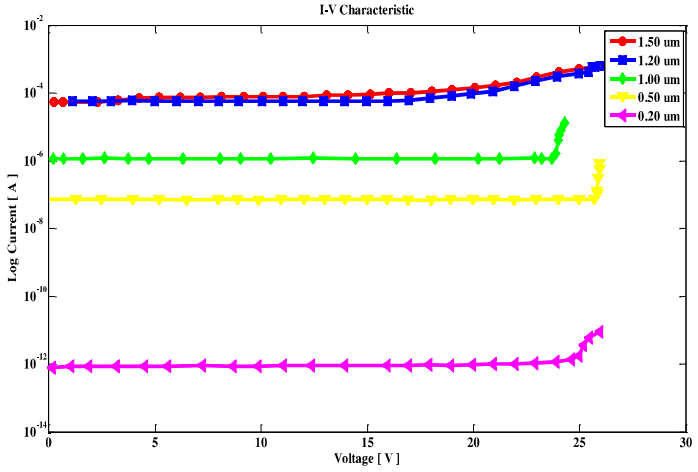

Figure 10: I-V characteristic of SAPD for various anode size

A high leakage current in SPAD without a guard ring may cause the device easily damage during the fabrication process. Thus, further optimization is performed on the device to obtain minimum leakage current by varying the anode size of SPAD. By changing the size of anode, the leakage current tends to decrease as the anode size is reduced as shown in Figure 1.10. In addition, the I-V characteristics of the proposed SPAD structure in the same agreement with

experimental results for fabricated SPAD in 1.8 V CMOS Process with various size of diffusion area in detecting the incoming photon [6, 15].

4.0 CONCLUSION

In this study, a Geiger mode SPAD has been successfully designed and simulated using Silvaco TCAD simulation tools. The process and device simulation characterization of SAPD are implemented to define the I-V characteristics with various doping concentration and the implantation of p-well layer as a guard ring. The doping levels of the n-well and p+ (p-diffusion) forming the avalanche breakdown p-n junction have also contributes to the higher V_{BD}, hence would decreasing the leakage current. From the simulation of breakdown with impact ionization, V_{BD} of 27 V and I_D less than 1 pA are obtained for a square shape SPAD with active area of 2 µm x 2 µm. The inclusion of guard ring layer on SPAD structure has shown that the premature breakdown is successfully prevented, where I_D of 0.85 pA with higher V_{BD}. By introducing the guard ring, the free carriers at the border of diode will be captured by the electric field, so that V_{BD} is increased and I_D is minimized. This would promise small dark count rate for photon counting application with this proposed SPAD device.

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